查询X3064102供应商

APPLICATION NOTE
A V A I L A B L E
3 or 4 Cell Li-Ion BATTERY PACKS

Preliminary Information

X3100

3 or 4 Cell Li-Ion Battery Protection and Monitor IC

FEATURE

- **Software selectable safety levels and variable protect detection/release times**
- **Integrated FET Drive Circuitry**
- **Cell voltage and current monitoring**
- **0.5% accurate voltage regulator**
- **Integrated 4kbit EEPROM**
- **Flexible Power Management with 1µA Sleep mode**
- **Cell balancing control**

BENEFIT

- **Optimize protection for chosen cells to allow maximum use of pack capacity.**
- **Reduce component count and cost**
- **Simplify implementation of fuel gauge**
- **Accurate voltage and current measurements**
- **Record battery history to optimize fuel gauge, track pack failures and monitor system use**
- **Reduce power to extend battery life**
- **Increase battery capacity and improve cycle life battery life**

DESCRIPTION

The X3100 is a protection and monitor IC for use in battery packs consisting of 3 or 4 Lithium-Ion battery cells. The device provides internal over-voltage, under-voltage, and over-current protection circuitry, internal EEPROM memory, an internal voltage regulator, and internal drive circuitry for switching external FET devices used to control cell charge, discharge, and cell voltage balancing.

Over-voltage, under-voltage, and over-current thresholds can be selected independently via software and stored in an internal non-volatile memory register. Detection and time-out delays can also be individually varied. Changes are made to the device via a 3MHz SPI serial interface.

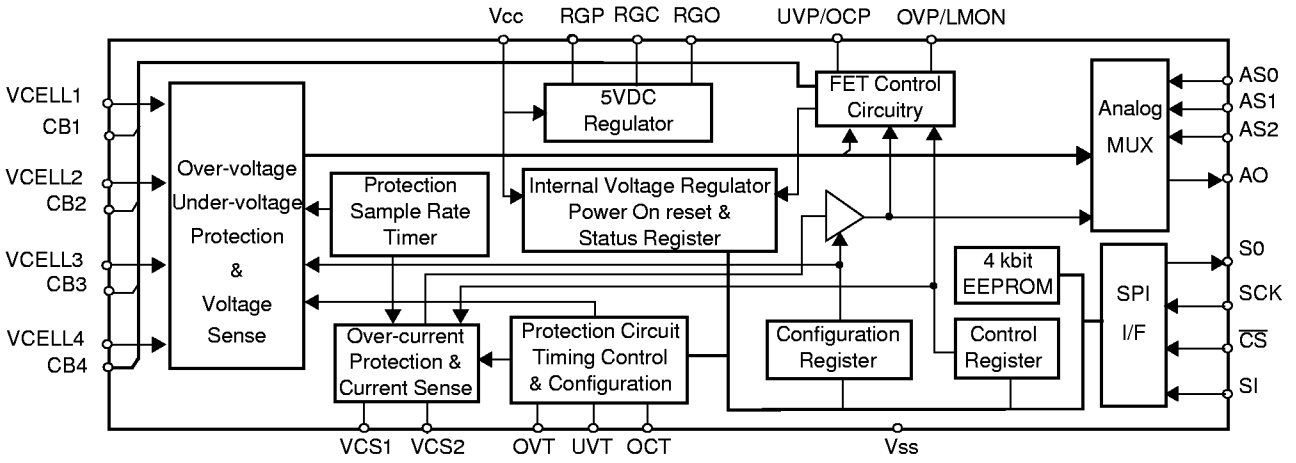
Using an internal analog multiplexer, the X3100 also allows battery parameters such as cell voltage and current (using a sense resistor) to be monitored externally. An off-board microcontroller and A/D converter can be used to implement fuel gauge and cell balancing functionality in software.

The X3100 contains a current sense amplifier. With selectable gains of 10, 25, 80 and 160, this circuit helps an external 10 bit A/D converter achieve better resolution than a more expensive 14 bit converter.

An internal 4kbit EEPROM memory featuring IDLock™, allows the designer to partition and “lock in” written battery cell/pack data.

The X3100 is housed in a 28 Pin SSOP and 28 Pin TSSOP package.

FUNCTIONAL DIAGRAM



©Xicor, Inc. 1994, 1995, 1996, 1997, 1998, 1999, 2000 Patents Pending

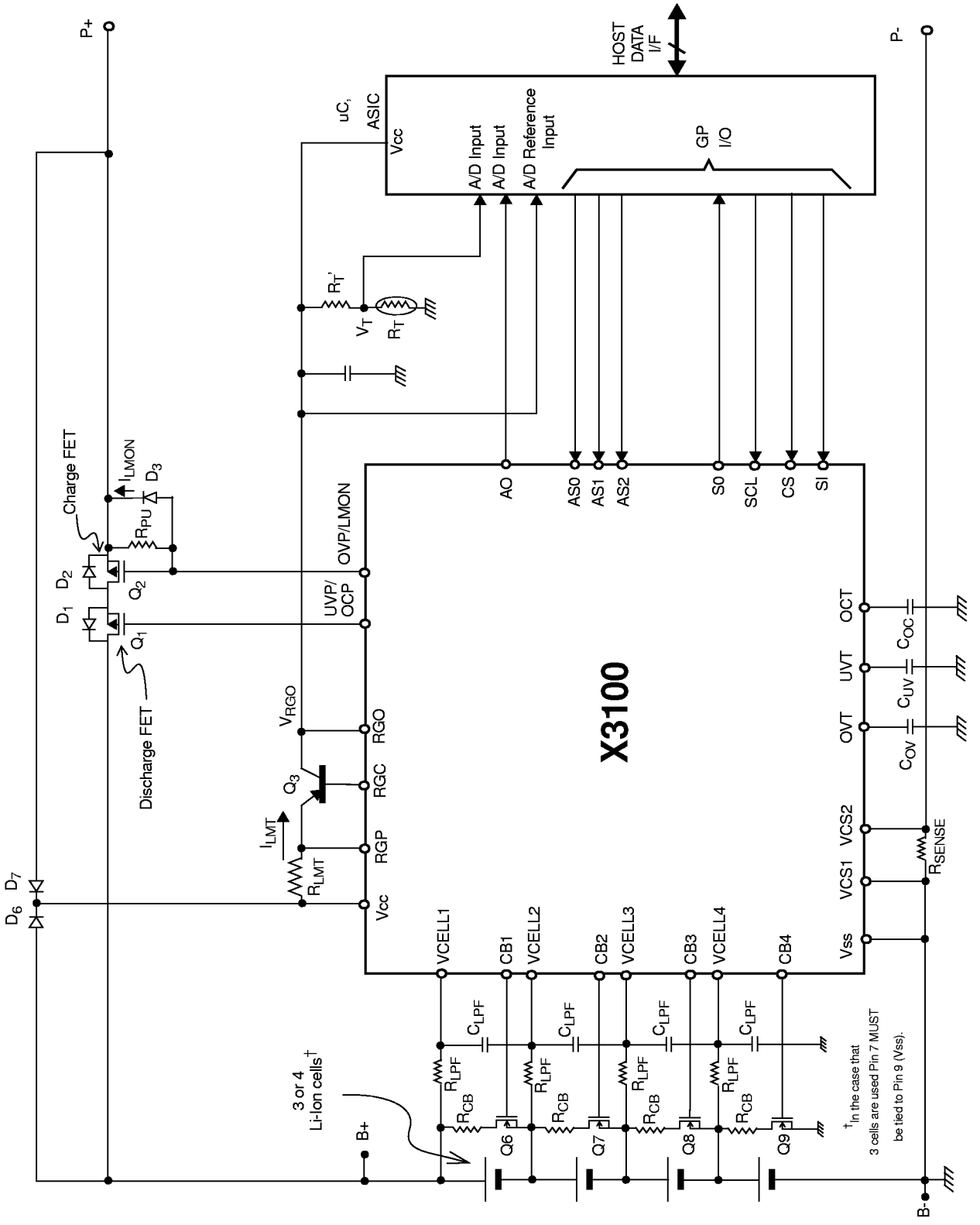


Figure 1. Typical Application Circuit

PRINCIPLES OF OPERATION

The X3100 provides two distinct levels of functionality and battery cell protection:

First, the device periodically monitors for over-voltage and under-voltage protection modes, while continuously monitoring for an over-current condition. A protection mode violation results from an over-voltage, under-voltage, or over-current state. The thresholds for these states are selected by the user through software.

Second, a microcontroller with A/D converter can measure battery cell voltages and current via pin AO and the on-board MUX of the X3100. The user can thus implement protection, charge/discharge, or fuel gauge software algorithms to suit the specific application and characteristics of the cells used. While monitoring these voltages, all protection circuits are monitored continuously.

All descriptions of the operation of the X3100 contained within this data sheet, are made with reference to the Typical Application Circuit shown in Figure 1.

The X3100 contains internal circuitry which enables the direct drive of MOSFET devices for power switching. As shown in Figure 1, pins UVP and OVP switch p-channel MOSFET's (Q_1 and Q_2) which control cell discharge and charge respectively. These devices shall be referred to as the "Discharge FET" and the "Charge FET". Since these FETs are p-channel devices, they will be ON when UVP/OCP or OVP/LMON are at level Vss, and OFF when UVP/OCP or OVP/LMON are at level Vcc.

These pins are switched ON/OFF under certain conditions in order to protect the battery cells from the damage which may occur in Over-voltage, Under-voltage, or Over-current states.

X3100 SPI SERIAL COMMUNICATION

The X3100 is designed to interface directly with the synchronous Serial Peripheral Interface (SPI) of many popular microcontroller families. This interface uses four signals, $\overline{CS}$, SCK, SI and SO. The signal $\overline{CS}$ when low, enables communications with the device. The SI pin carries the input signal and SO provides the output signal. SCK clocks data in or out. The X3100 operates in SPI mode 0 which requires SCK to be normally low when not transferring data. It also specifies that the rising edge of SCK clocks data into the device, while the falling edge of SCK clocks data out.

This SPI port is used to set the various internal registers, write to the EEPROM array, and select various device functions.

The X3100 contains an 8-bit instruction register. It is accessed by clocking data into the SI input. $\overline{CS}$ must be LOW during the entire operation. Table 1 contains a list of the instructions and their opcodes. All instructions, addresses and data are transferred MSB first.

Table 1. X3100 Instruction Set

Instruction Name	Instruction Format*	Description
WREN	0000 0110	Set the Write Enable Latch (Write Enable Operation) - Figure 16
WRDI	0000 0100	Reset the Write Enable Latch (Write Disable Operation) - Figure 16
EEWRITE	0000 0010	Write operation followed by address and data (For 4kbit EEPROM) - Figures 20,21
EEREAD	0000 0011	Read operation followed by address (For 4kbit EEPROM) - Figure 18
WCFIG	0000 1001	Write to Configuration Register (Followed by two bytes of data - Figures 3,13). Data stored in SRAM only and will power-up to previous settings (Figures 2,4)
WCNTR	0000 1010	Write to Control Register (Followed by two bytes of data) - Figure 3
RDSTAT	0000 1011	Read contents of Status Register - Figure 15
SET IDL	0000 0001	Set EEPROM ID Lock Partition (Followed by Partition Byte) - Figure 17
EEREAD STAT	0000 0101	Reads IDLock settings & status of EEPROM EEWRITE Instruction - Figure 19

*Instructions are shown with MSB in leftmost position. Instructions are transferred MSB first.

Table 2. Configuration Register Functionality

Bit(s)	Name	Function
0-5	-	(Don't Care)
6	SWCEN	Switch cell Charge Enable threshold function ON/OFF
7	CELLN	Set the Number of Li-Ion battery Cells used (3 or 4)
8-9	VCE1-VCE0	Select Cell Charge threshold Voltage
10-11	VOC1-VOC0	Select Over-current threshold Voltage
12-13	VUV1-VUV0	Select Under-voltage threshold Voltage
14-15	VOV1-VOV0	Select Over-voltage threshold Voltage

Data input is sampled on the first rising edge of SCK after $\overline{CS}$ goes LOW. SCK is static, allowing the user to stop the clock and then start it again to resume operations where left off.

CONFIGURATION REGISTER

The X3100 can be configured for specific user requirements using the Configuration Register.

The Configuration Register is realized as two bytes of NOVRAM memory. This memory features a high-speed static RAM (SRAM) overlaid bit-for-bit with non-volatile "Shadow" EEPROM. An automatic array recall operation reloads the contents of the shadow EEPROM into the SRAM Configuration Register upon power-up (Figure 2).

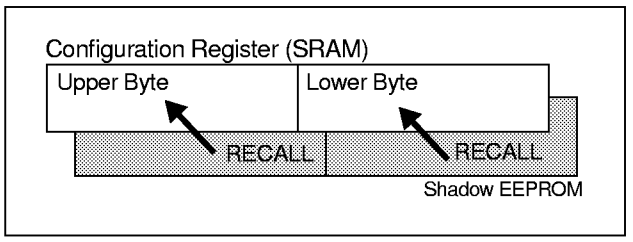


Figure 2. Power up of Configuration Register.

The Configuration Register is designed for unlimited write operations to SRAM, and a minimum of 1,000,000 store operations to the EEPROM. Data retention is specified to be greater than 100 years.

The Configuration Register consists of two bytes (upper and lower) of data (Tables 4, 5).

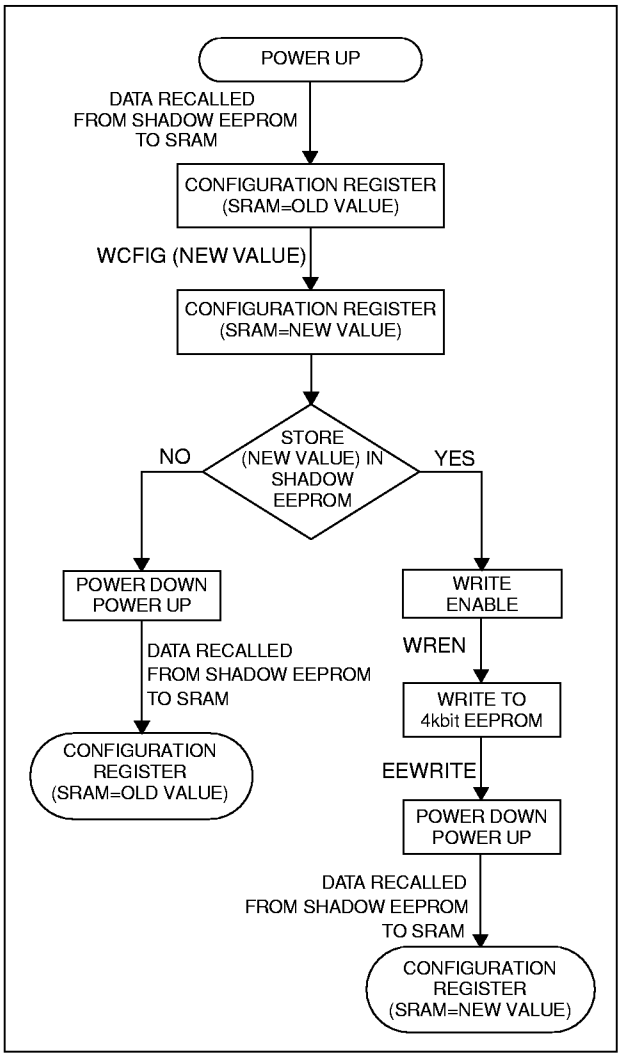


Figure 3. Writing to Configuration Register.

Table 3. Control Register Functionality

Bit(s)	Name	Function
0-4	-	(Don't Care)
5-6	0, 0	Reserved—write 0 to these locations.
7	SLP	Select X3100 Sleep mode.
8-9	CSG1-CSG0	Select current sense voltage gain
10	OVPC	OVP Control: Switch pin OVP = Vcc/Vss
11	UVPC	UVP Control: Switch pin UVP = Vcc/Vss
12	CBC1	CB1 Control: Switch pin CB1 = Vcc/Vss
13	CBC2	CB2 Control: Switch pin CB2 = Vcc/Vss
14	CBC3	CB3 Control: Switch pin CB3 = Vcc/Vss
15	CBC4	CB4 Control: Switch pin CB4 = Vcc/Vss

Table 4. Configuration Register—Upper Byte

15	14	13	12	11	10	9	8
VOV1	VOV0	VUV1	VUV0	VOC1	VOC0	VCE1	VCE0

Table 5. Configuration Register—Lower Byte

7	6	5	4	3	2	1	0
CELLN	SWCEN	x	x	x	x	x	x

The Configuration Register can be written, by first writing the WCFIG Instruction on the SI pin, followed by two bytes of data (Figure 14). The quantities that can be set in the Configuration Register are listed in Table 2.

It should be noted that the bits of the shadow EEPROM are for the dedicated use of the Configuration Register, and are NOT part of the general purpose 4kbit EEPROM array.

After writing to this register using a WCFIG Instruction, data will be stored only in the SRAM of the Configuration Register. In order to store data in shadow EEPROM, a WREN Instruction (Figure 17), followed by a EEWRITE to any address of the 4kbit EEPROM memory array must occur (Figure 21). This sequence initiates an internal nonvolatile write cycle which permits data to be stored in the shadow EEPROM cells. It must be noted that even though a EEWRITE is made to the general purpose 4kbit EEPROM array, the value and address to which it is written, is unimportant. If this procedure is not followed, the Configuration Register will power up to the last previously stored values following a power down sequence (Figure 3).

The default settings of the Configuration Register (at shipping) are 37h and C0h for the upper and lower bytes respectively.

CONTROL REGISTER

The Control Register is realized as two bytes of volatile RAM (Table 6, 7). This register can be written to by first issuing the WCNTR Instruction on SI, followed by two bytes of the Control Register data (Figure 15).

Table 6. Control Register—Upper Byte

15	14	13	12	11	10	9	8
CBC4	CBC3	CBC2	CBC1	UVPC	OVPC	CSG1	CSG0

Table 7. Control Register—Lower Byte

7	6	5	4	3	2	1	0
SLP	0	0	x	x	x	x	x

Since the Control Register is realized in Volatile memory, data will be lost following a power down and power up sequence. The default value of the Control Register on initial power up or when exiting the SLEEP MODE is 00h (for both upper and lower bytes respectively). The functions that can be manipulated by the Control Register are shown in Table 3.

Table 8. Status Register Functionality.

Bit(s)	Name	Description	Case	Status	Interpretation
0	VRGS+OCDS	Voltage Regulator Status + Over Current Detection Status	-	1	V_{RGO} not yet tuned (V_{RGO}=5V ± 10%) **OR** X3100 in Over-current protection mode.
				0	V_{RGO} tuned (V_{RGO}=5V ± 0.5%) **AND** X3100 NOT in Over-current protection mode.
1	UVDS	Under Voltage Detection Status	-	1	X3100 in Under-voltage protection mode
				0	X3100 NOT in Under-voltage protection mode
2	CCES+OVDS	Cell Charge Enable Status + Over Voltage Detection Status	SWCEN =0†	1	$V_{CELL} < V_{CE}$ **OR** X3100 in Over-voltage protection mode
				0	$V_{CELL} > V_{CE}$ **AND** X3100 NOT in Over-voltage protection mode
			SWCEN =1†	1	X3100 in Over-voltage protection mode
				0	X3100 NOT in Over-voltage protection mode
3–7	-		-	0	Not Used (Always return zero)

† This bit is set in the Configuration Register.

STATUS REGISTER

The status of the X3100 can be verified by reading the contents of the Status Register (Table 9).

Table 9. Status Register.

7	6	5	4	3	2	1	0
0	0	0	0	0	CCES+ OVDS	UVDS	VRGS+ OCDS

The function of each bit in the Status Register is shown in Table 8.

Bit 0 of the Status Register (VRGS+OCDS) actually indicates the status of two conditions of the X3100. VRGS (Voltage Regulator Status) is an internally generated signal which indicates that the output of the voltage regulator (VRGO) has reached an output of 5VDC ± 0.5%. In this case, the voltage regulator is said to be “tuned”. Before the signal VRGS goes low (i.e. before the voltage regulator is tuned), the voltage at the output of the regulator is nominally 5VDC ± 10% (See Section "Voltage Regulator Control" on page 21) Over Current Detection Status (OCDS) is another internally generated signal which indicates whether or not the X3100 is in Over-current protection mode.

Signals VRGS and OCDS are logically OR’ed together (VRGS+OCDS) and written to bit 0 of the Status register (See Tables 8, 9 and Figure 4).

Bit 1 of the Status Register, simply indicates whether or not the X3100 is in Under-voltage protection mode.

Bit 2 of the Status Register (CCES+OVDS) also indicates the status of two conditions of the X3100, depending upon the status of SWCEN (Bit 6 of the Configuration Register—See Section "Configuration Register" on page 4. Also see Section “ Sleep Mode” on page 17). CCES (Cell Charge Enable Status) is an internally generated signal which indicates the status of any cell voltage (V_{CELL}), with respect to the Cell Charge Enable Voltage (V_{CE}). OVDS (Over-Voltage Detection Status) is an internally generated signal which indicates whether or not the X3100 is in Over-voltage protection mode.

When Cell Charge Enable function is switched ON (Configuration Bit SWCEN=0), then the signals CCES and OVDS are logically OR’ed (CCES+OVDS) and written to bit 2 of the Status Register. If the Cell Charge Enable function is switched OFF (Configuration Bit SWCEN=1), then bit 2 of the Status Register effectively only represents information about the Over-Voltage Status (OVDS) of the X3100 (See Tables 8, 9 and Figure 5).

POWER ON SEQUENCE

Initial connection of the Li-Ion cells in the battery pack will not power up the battery pack. Instead, the X3100 enters and remains in the SLEEP mode. To exit the SLEEP mode, after the initial power up sequence, or following any other SLEEP MODE, a minimum of 14V (V_{SLR}) is applied to the V_{CC} pin, as would be the case during a battery charge condition. When V_{SLR} is applied to V_{CC}, the analog select pins (AS2-AS0) must be low, so the X3100 powers up correctly into the Normal Operating Mode.

When entering the Normal Operating Mode, either from initial power up or following the SLEEP MODE, all bits in the control register are zero. With UVPC and OVPC bits at zero, the charge and discharge FETs are off. The microcontroller must turn these on to activate the pack. The microcontroller would typically check voltage and current level prior to turning on the FETs.

As soon as the VRGS + OCDS bit goes to zero after exiting the sleep mode, the processor can change the AS bits to begin reading selected analog voltages.

When exiting the sleep mode in subsequent operations, without powering down the pack, the device operates identically to the initial power up sequence and requires the AS2:AS0 pins to be low. See Figure 6.

After the X3100 “wakes up” , data can be read from the X3100 via the SPI port after time t_{PUR} (Power-up to read operation). The Status Register can be read out on pin SO after first issuing the RDSTAT Instruction on pin SI (Figure 16). It should be noted however, that if the microcontroller used is being powered via pin RGO, then the output voltage (V_{RGO}) will not be tuned to 5VDC ± 0.5% until a nominal time of T_{OC} (Over-current detection time) + 2ms (Figure 4, 5).

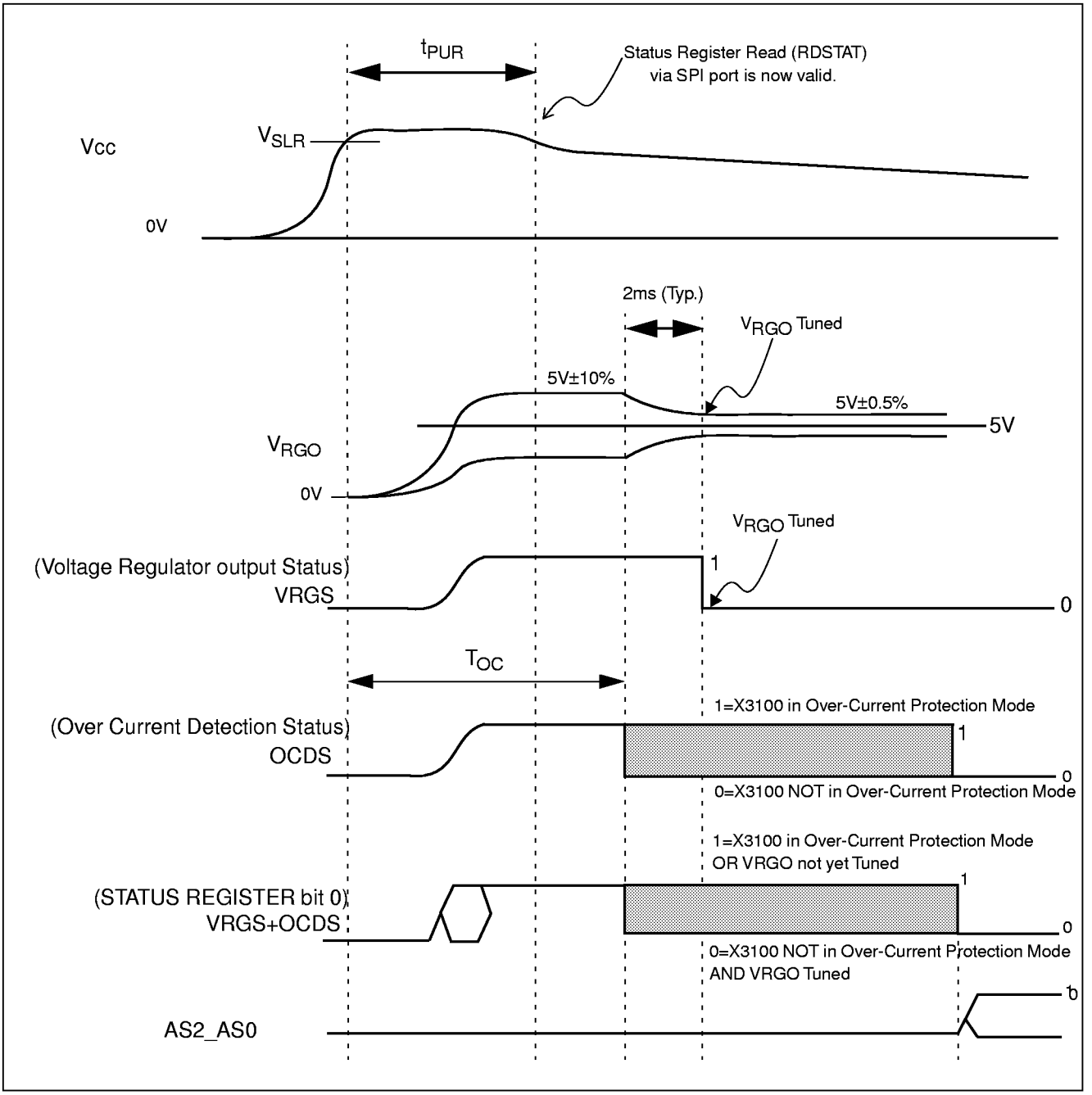


Figure 4. Status Register, Bit 0—Timing Diagram.

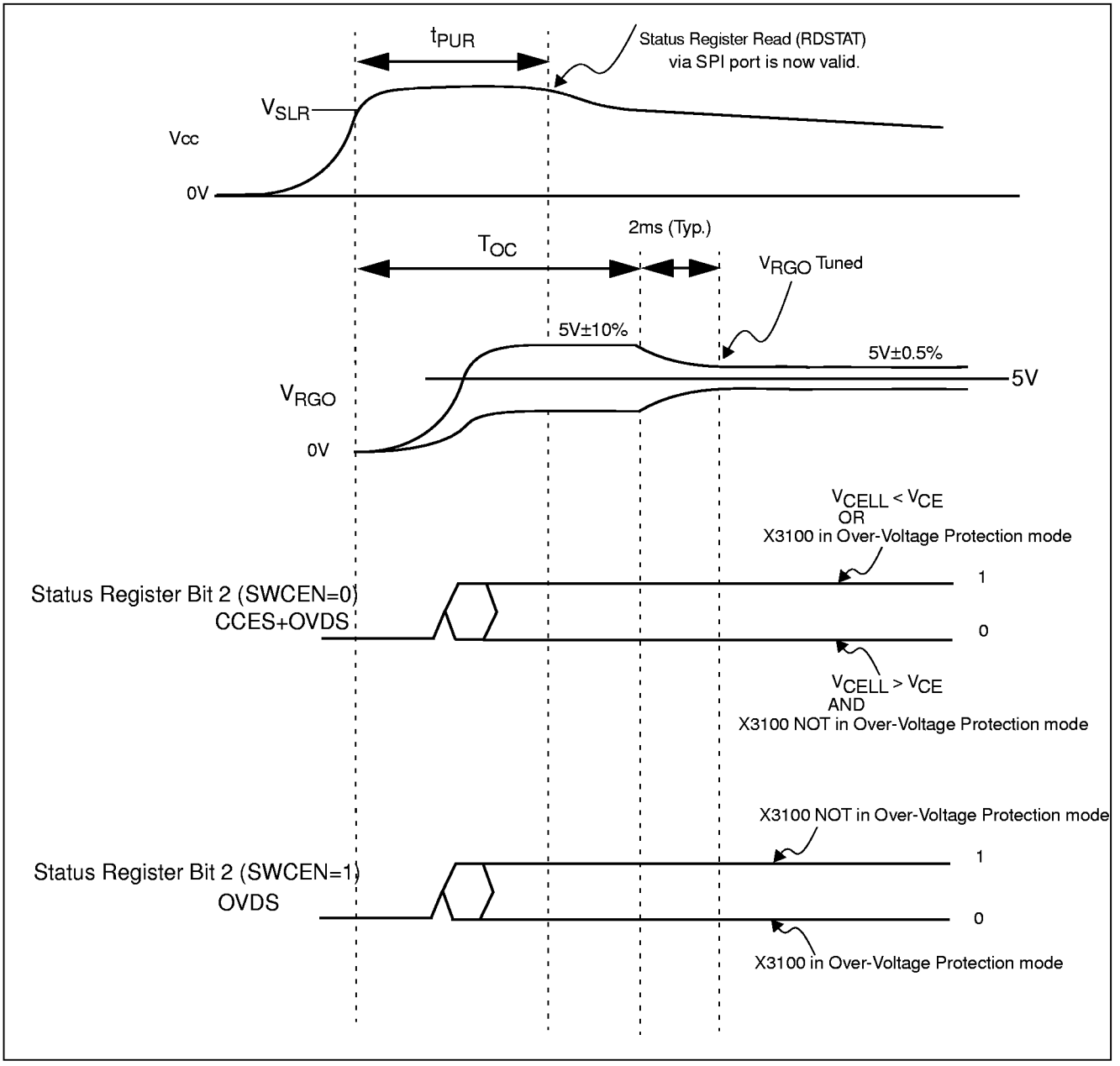


Figure 5. Status Register, Bit 2—Timing Diagram.

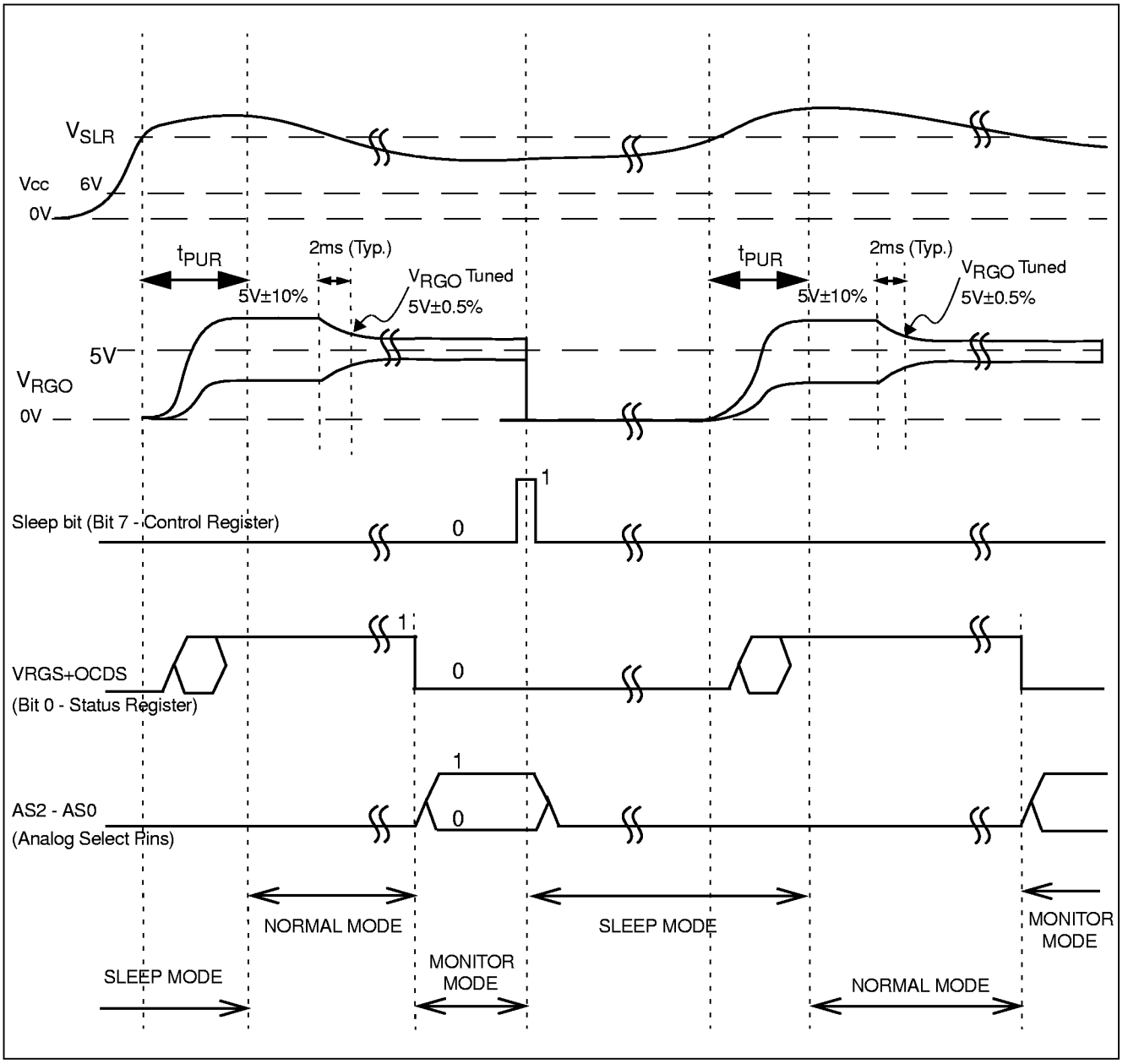


Figure 6. Power up and Sleep Mode Timing.

X3100 INTERNAL PROTECTION FUNCTIONS

The X3100 provides periodic monitoring (see Section "Periodic Protection Monitoring" on page16) for Over-Voltage and Under-Voltage states and continuous monitoring for an Over-current state. It has automatic shutdown when a protection mode is encountered, as well as automatic return after the device is released from a protection mode. When sampling voltages through the analog port (Monitor Mode), Over-Voltage and Under-Voltage protection monitoring is also performed on a continuous basis.

Voltage thresholds for each of these protection modes (V_{OV}, V_{UV}, and V_{OC} respectively) can be individually selected via software and stored in an internal non-volatile register. This feature allows the user to avoid the restrictions of mask programmed voltage thresholds, and is especially useful during prototype/evaluation design stages or when cells with slightly different charcteristics are used in an existing design.

Delay times for the detection of, and release from protection modes (T_{OV}, T_{UV}/T_{UVR}, and T_{OC}/T_{OCR} respectively) can be individually varied by setting the values of external capacitors connected to pins OVT, UVT, OCT.

Over-Voltage Protection

The X3100 monitors the voltage on each battery cell (V_{CELL}). If for any cell, $V_{CELL} > V_{OV}$ for a time exceeding T_{OV}, then the Charge FET will be switched OFF (OVP/LMON=V_{CC}). The device has now entered Over-voltage protection mode (Figure 7). The status of the Discharge FET (via pin UVP) will remain unaffected.

While in Over-voltage protection mode, it is possible to change the state of the OVPC bit in the Control Register such that OVP/LMON=Vss (Charge FET=ON). Although the OVPC bit in the Control register can be changed, the change will not be seen at pin OVP until the X3100 returns from Over-voltage protection mode.

The Over-voltage detection delay T_{OV}, is varied using a capacitor (C_{OV}) connected between pin OVT and GND. A typical delay time is shown in Table 10. The delay T_{OV} that results from a particular capacitance C_{OV}, can be approximated by the following linear equation:

$$T_{OV}\,(s) \approx 10 \times C_{OV}\,(\mu F).$$

Table 10. Typical Over-voltage detection time

Symbol	C_{OV}	Delay
T_{OV}	0.1µF	1.0s (Typ)

The device further continues to monitor the battery cell voltages, and is released from over-voltage protection mode when $V_{CELL} < V_{OVR}$, for all cells. When the X3100 is released from over-voltage protection mode, the Charge FET is automatically switched ON (OVP/LMON=V_{SS}). When the device returns from Over-voltage protection mode, the status of the Discharge FET (pin UVP/OCP) remains unaffected.

The value of V_{OV} can be selected from the values shown in Table 11 by setting bits VOV1, VOV0 in the Configuration Register. The WCFIG instruction must first be issued on SI, followed by bits VOV1, VOV0, and the remaining two bytes of the Configuration Register (Table 1, Figure 14).

Table 11. Over-Voltage Threshold Voltage Selection.

Configuration Register Bits		
VOV1	VOV0	Operation
0	0	V_{OV}=4.20V
0	1	V_{OV}=4.25V
1	0	V_{OV}=4.30V
1	1	V_{OV}=4.35V

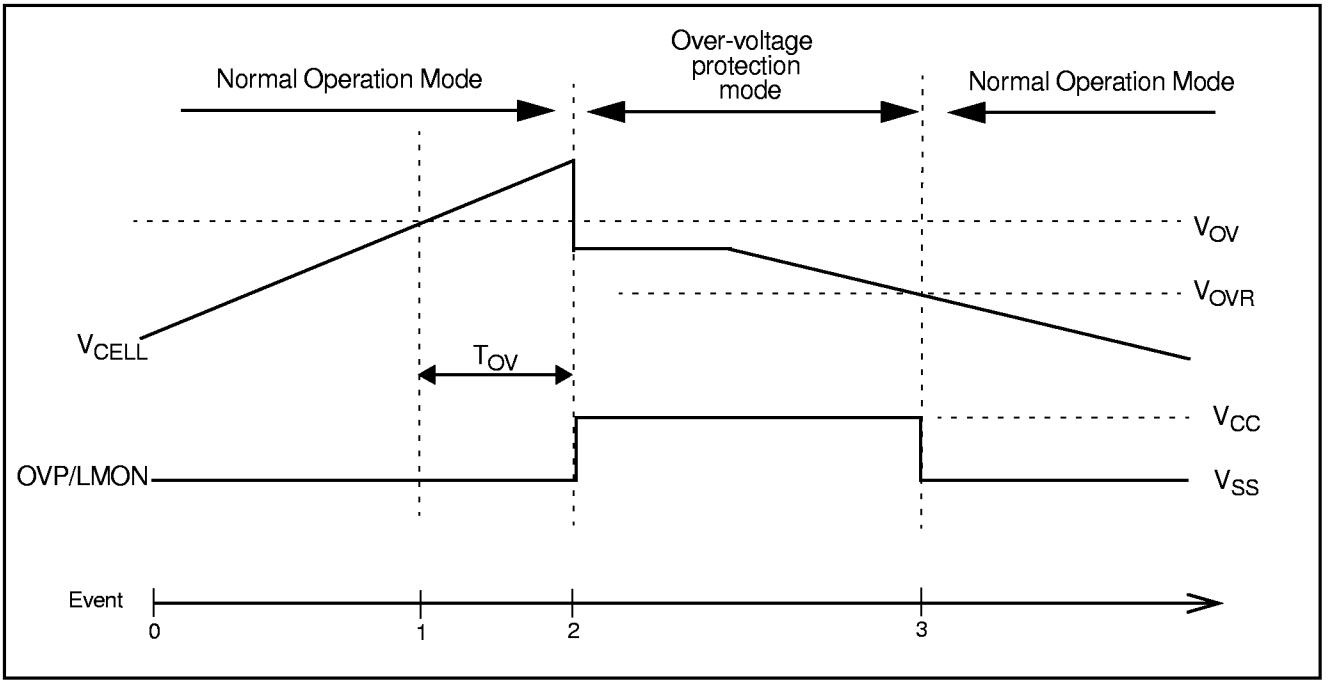


Figure 7. Over-Voltage Protection Mode—Event Diagram

Table 12. Over-Voltage Protection Mode—Event Diagram Description

Event	Event Description
[0,1)	— Discharge FET is ON (UVP/OCP=Vss). — Charge FET is ON (OVP/LMON=Vss), and hence battery cells are permitted to receive charge. — All cell voltages (V_{CELL}-V_{CELL4}) are below the Over-voltage Threshold voltage (V_{OV}). — The device is in Normal Operation Mode (i.e. not in a Protection mode).
[1]	— The voltage of one or more of the battery cells (V_{CELL}), exceeds V_{OV}. — The internal Over-voltage detection delay timer begins counting down. — The device is still in Normal Operation Mode
(1,2)	The internal Over-voltage detection delay timer continues counting for T_{OV} seconds.
[2]	The internal Over-voltage detection delay timer times out **AND** V_{CELL} still exceeds V_{OV}. — Therefore, the internal Over-voltage sense circuitry switches the Charge FET OFF (OVP/LMON=Vcc). — The device has now entered Over-Voltage protection mode.
(2,3)	While in Over-voltage protection mode: — The battery cells are permitted to discharge via the Discharge FET, and Diode D_2 across the Charge FET — The X3100 monitors the voltages V_{CELL1}-V_{CELL4} to determine whether or not they have all fallen below the “Return from Over-Voltage threshold” (V_{OVR}). — (It is possible to change the status of UVP/OCP or OVP/LMON using the Control Register)
[3]	— All cell voltages fall below V_{OVR}—The device is now in Normal Operation mode. — The X3100 automatically switches Charge FET=ON (OVP/LMON=Vss) — The status of the Discharge FET remains unaffected.
[4]	— Charging of the battery cells can now resume.

Under-Voltage Protection

If $V_{CELL} < V_{UV}$, for a time exceeding T_{UV}, the cells are said to be in a under-voltage state (Figure 8). In this instance, the X3100 automatically switches the Discharge FET OFF (UVP/OCP=Vcc), and then enters Sleep mode (Section "SLEEP MODE" on page 20).

In order for the X3100 to enable battery cell discharge once more, the following steps must occur:

- The X3100 must wake from Sleep mode (Section "SLEEP MODE" on page 20).
- The Charge FET must be switched ON (OVP/LMON=Vss), via the Control register (Section "Control Register" on page 5).

All battery cells must satisfy the condition: $V_{CELL} > V_{UVR}$ for a time exceeding T_{UVR}.

The times T_{UV}/T_{UVR} are varied using a capacitor (C_{UV}) connected between pin UVT and GND (Table 13). The delay T_{UV} that results from a particular capacitance C_{UV}, can be approximated by the following linear equation:

$$T_{UV}\ (s) \approx 10 \times C_{UV}\ (\mu F)$$

$$T_{UVR}\ (ms) \approx 70 \times C_{UV}\ (\mu F)$$

The value of V_{UV} can selected from the values shown in Table 14, by setting bits VUV1, VUV0 in the Configuration.

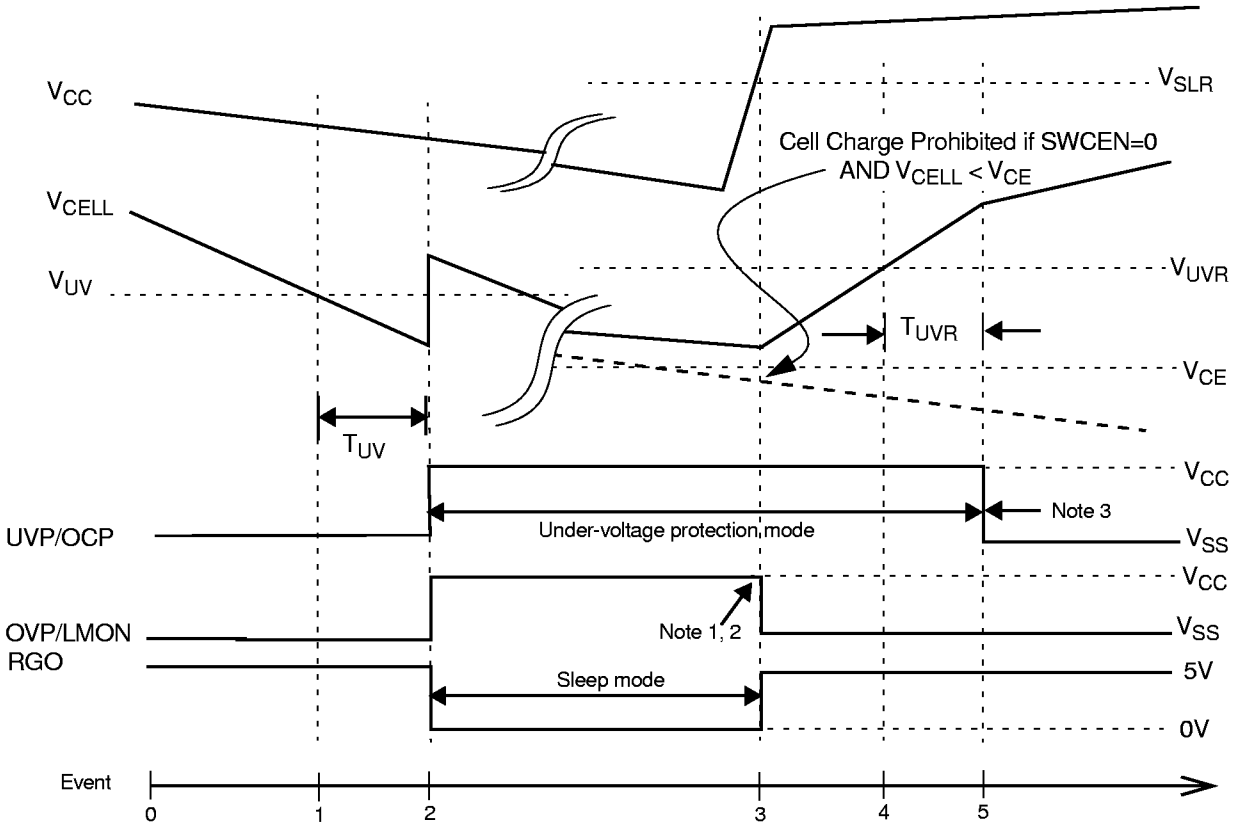
Table 13. Typical Under-Voltage delay times.

Symbol	Description	C_{UV}	Delay
T_{UV}	Under-voltage detection delay	0.1µF	1.0s (Typ)
T_{UVR}	Under-voltage release time	0.1µF	7ms (Typ)

Register. The WCFIG instruction must first be issued on SI, followed by bits VUV1, VUV0, and the remaining two bytes of the Configuration Register.

Table 14. Under-Voltage Threshold Voltage Selection.

Configuration Register Bits		
VUV1	VUV0	Operation
0	0	V_{UV}=1.95V
0	1	V_{UV}=2.05V
1	0	V_{UV}=2.15V
1	1	V_{UV}=2.25V



Note 1: If SWEN=0 and $V_{CELL} < V_{CE}$, then OVP/LMON stays high and charging is prohibited.

Note 2: OVP/LMON stays high until the microcontroller writes a "1" to the OVPC bit in the control register. This sets the signal low, which turns on the charge FET. It cannot be turned on prior to this time.

Note 3: UVP/OCP stays high until the microcontroller writes a "1" to the UVPC bit in the control register. This sets the signal low, which turns on the discharge FET. 14It cannot be turned on prior to this time.

Figure 8. Under-Voltage Protection Mode—Event Diagram

Table 15. Under-Voltage Protection Mode—Event Diagram Description

Event	Event Description
[0,1)	— Charge FET is ON (OVP/LMON=Vss) — Discharge FET is ON (UVP/OCP=Vss), and hence battery cells are permitted to discharge. — All cell voltages ($VCELL_1$-$VCELL_4$) are above the Under-voltage Threshold voltage (V_{UV}). — The device is in Normal Operation Mode (i.e. not in a Protection mode).
[1]	— The voltage of one or more of the battery cells (V_{CELL}), falls below V_{UV}. — The internal Under-voltage detection delay timer begins counting down. — The device is still in Normal Operation Mode
(1,2)	The internal Under-voltage detection delay timer continues counting for T_{UV} seconds.
[2]	— The internal Under-voltage detection delay timer times out, AND V_{CELL} is still below V_{UV}. — The internal Over-voltage sense circuitry switches the Discharge FET OFF (UVP/OCP=Vcc). — The device has now entered Under-Voltage protection mode. — At the same time, the device also enters Sleep mode (See Section "SLEEP MODE" on page 20).

Table 15. Under-Voltage Protection Mode—Event Diagram Description (Continued)

Event	Event Description	
(2,3)	While device is in Sleep (in Under-Voltage protection) mode: — The Charge FET is switched OFF (OVP/LMON=Vcc). — The power to ALL internal circuitry is switched OFF. Power consumption is limited to less than 1µA. — The output of the 5VDC voltage regulator (RGO) is 0V. — Access to the X3100 via the SPI port is NOT possible.	
[3]	Return from Sleep mode (but still in Under-Voltage protection mode): — Vcc rises about the "Return from Sleep mode threshold Voltage" (V_{SLR})—This would normally occur in the case that the battery pack was connected to a charger. The X3100 is now powered via P+/P-, and not the battery pack cells. — Power is returned to ALL internal circuitry — 5VDC output is returned to the regulator output (RGO). — Access is enabled to the X3100 via the SPI port. — The status of the Discharge FET remains OFF (It is possible to change the status of UVPC in the Control Register, although it will have no effect at this time).	
(3,4)	If the cell Charge Enable Function is switched ON AND $V_{CELL} > V_{CE}$ **OR** Charge Enable Function is switched OFF	— The Charge FET is switched On (OVP/LMON=Vss) by the microcontroller by writing a "1" to the OVPC bit in the Control Register. — The battery cells now receive charge via the Charge FET and diode D1 across the Discharge FET (which is OFF). — The X3100 monitors the voltages V_{CELL} to determine whether or not it has risen above V_{UVR}.
	If the cell Charge Enable Function is switched ON **AND** $V_{CELL} < V_{CE}$	— Charge / Discharge of the battery cells via P+ is no longer permitted (Charge FET and Discharge FET are held OFF). — (Charging may re-commence only when SWCE bit - See Sections: "Configuration Register" page 4, and "Sleep mode" page 17 - is switched OFF)
[4]	— The voltage of all of the battery cells (V_{CELL}), have risen above V_{UVR}. — The internal Under-voltage release timer begins counting down. — The X3100 is still in Under-Voltage protection mode.	
(4,5)	The internal Under-voltage Release timer continues counting for T_{UVR} seconds. The X3100 should be in Monitor Mode (AS2:AS0 not all low) for recovery time based on t_{UVR}. Otherwise recovery is based on two successive samples about 120ms apart.	
[5]	— The internal Under-voltage release timer times out, AND V_{CELL} is still above V_{UVR}. — The device returns from Under-voltage protection mode, and is now in Normal Operation mode. — The Discharge FET is can now be switched ON (UVP/OCP=Vss) by the microcontroller by writing a "1" to the UVPC bit of the control register. — The status of the Charge FET remains unaffected (ON) — The battery cells continue to receive charge via the Charge FET and Discharge FET (both ON).	

Over-Current Protection

In addition to monitoring the battery cell voltages, the X3100 continually monitors the voltage VCS_{21} (VCS_2–VCS_1) across the current sense resistor (R_{SENSE}). If $VCS_{21} > V_{OC}$ for a time exceeding T_{OC}, then the device enters over-current protection mode (Figure 10). In this mode, the X3100 automatically switches the Discharge FET OFF (UVP/OCP=Vcc) and hence prevents current from flowing through the battery terminals (Figure 1: P+ and P-).

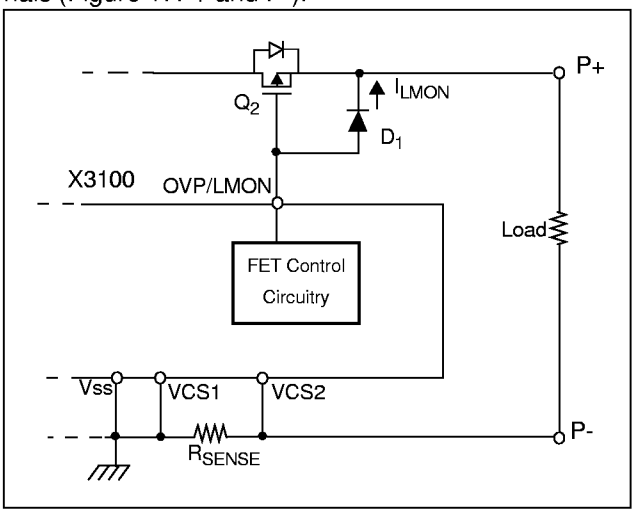


Figure 9. Over-Current Protection

The 5VDC voltage regulator output (V_{RGO}) is always active during an Over-current protection mode.

Once the device enters over-current protection mode, the X3100 then begins a Load Monitor state. In the Load Monitor state, a small current (I_{LMON}=7.5µA typ.) is passed out of pin OVP/LMON in order to determine the Load resistance. The Load Resistance is the impedance seen looking out of pin OVP/LMON, between terminal P+ and pin Vss (Figure 1, Figure 9).

If the Load Resistance is not a short (i.e. > 150kΩ), then the device returns from the Load Monitor state (I_{LMON}=0µA). If the Load Resistance > 150kΩ (I_{LMON}=0µA) for a time exceeding T_{OCR}, then the X3100 is released from over-current protection mode. The Discharge FET is then automatically switched ON (UVP/OCP=Vss) by the X3100. This is unless the status of UVP/OCP has been changed in Control Register (by manipulating bit UVPC) during the Over-current protection mode.

T_{OC}/T_{OCR} are varied using a capacitor (C_{OC}) connected between pin OCT and GND. A list of typical delay times is shown in Table 16. Note that the value C_{OC} should be larger than 1nF.

The delay T_{OC} and T_{OCR} that results from a particular capacitance C_{OC}, can be approximated by the following equations:

$$T_{OC}\ (ms) \approx 10 \times C_{OC}\ (nF)$$

$$T_{OCR}\ (ms) \approx 10 \times C_{OC}\ (nF)$$

Table 16. Typical Over-current delay times.

Symbol	Description	C_{OC}	Delay
T_{OC}	Over-current detection delay	1nF	10ms (Typ)
T_{OCR}	Over-current release time	1nF	10ms (Typ)

The value of V_{OC} can be selected from the values shown in Table 17, by setting bits VOC1, VOC0 in the Configuration Register. The WNFIG instruction must first be issued on SI, followed by bits VOC1, VOC0, and the remaining two bytes of the Configuration Register.

Table 17. Over-Current Threshold Voltage Selection.

Configuration Register Bits		
VOC1	VOC0	Operation
0	0	V_{OC}=0.075V
0	1	V_{OC}=0.100V
1	0	V_{OC}=0.125V
1	1	V_{OC}=0.150V

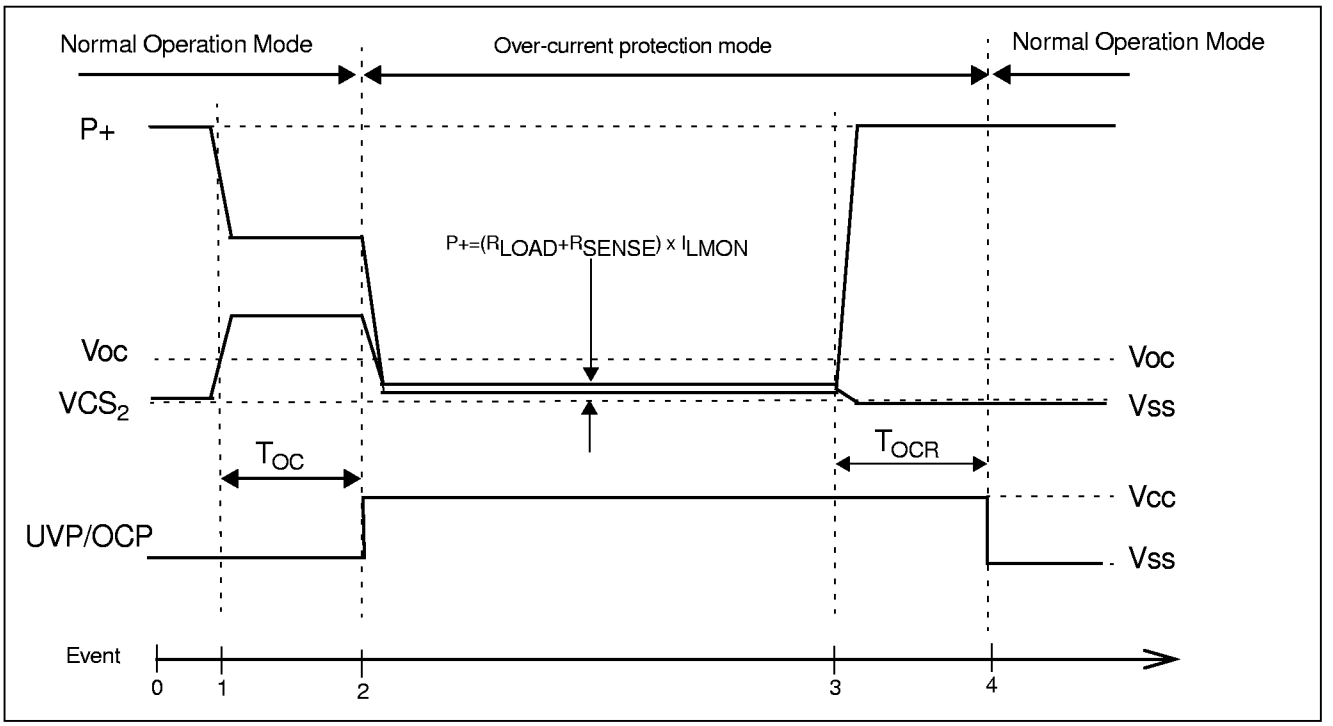


Figure 10. Over-Current Protection Mode—Event Diagram

Table 18. Over-current Protection Mode—Event Diagram Description

Event	Event Description
[0,1)	— Discharge FET is ON (OCP=Vss). Battery cells are permitted to discharge. — VCS_{21} (VCS_2–VCS_1) is less than the Over-current Threshold voltage (V_{OC}). — The device is in Normal Operation Mode (i.e. not in a Protection mode).
[1]	— A short-circuit occurs between the battery terminals P+ and P- (Figure 1, Figure10). — The positive battery terminal voltage (P+) falls, and VCS_{21} exceeds V_{OC}. — The internal Over-current detection delay timer begins counting down. — The device is still in Normal Operation Mode
(1,2)	The internal Over-current detection delay timer continues counting for T_{OC} seconds.
[2]	— The internal Over current detection delay timer times out, AND VCS_{21} is still above V_{OC}. — The internal Over-voltage sense circuitry switches the Discharge FET OFF (UVP/OCP=Vcc). — The device now begins a Load Monitor state by passing a small test current (I_{LMON}=7.5µA) out of pin OVP/LMON. This senses if a short circuit (i.e. if the Load resistance < 150kΩ) still exists across P+/P-. — The device has now entered Over current protection mode. — It is possible to change the status of UVPC and OVPC in the Control Register, although the status of pins UVP/OCP and OVP/LMON will not change until the device has returned from Over-current protection mode.
(2,3)	— The X3100 now continuously monitors the Load resistance to detect whether or not a short circuit is still present across the battery terminals P+/P-.

Table 18. Over-current Protection Mode—Event Diagram Description (Continued)

Event	Event Description
[3]	— The device detects the Load resistance has risen above 250kΩ. — Voltages P+ and VCS_{21} return to their normal levels. — The test current from pin OVP/LMON is stopped (I_{LMON}=0µA) — The device has now returned from the Load Monitor state — The internal Over-current release time timer begins counting down. — Device is still in Over-current protection mode.
(3,4)	The internal Over-current release timer continues counting for T_{OCR} seconds.
[4]	— The internal Over-current release timer times out, AND VCS_{21} is still below V_{OC}. — The device returns from Over-current protection mode, and is now in Normal Operation mode. — The Discharge FET is automatically switched ON (UVP/OCP=Vss)—unless the status of UVPC has been changed in the Control Register during the Over-current protection mode. — The status of the Charge FET remains unaffected. — Discharge of the battery cells is once again possible.

MONITOR MODE

Analog Multiplexer Selection

The X3100 can be used to externally monitor individual battery cell voltages, and battery current. Each quantity can be monitored at the analog output pin (AO), and is selected using the analog select (AS0–AS2) pins (Table 19).

Table 19. AO selection map

AS			AO output
2	1	0	
L	L	L	Vss(1)
L	L	H	VCELL1–VCELL2 ($VCELL_{12}$)
L	H	L	VCELL2–VCELL3 ($VCELL_{23}$)
L	H	H	VCELL3–VCELL4 ($VCELL_{34}$)
H	L	L	VCELL4–Vss ($VCELL_4$)
H	L	H	VCS1–VCS2 (VCS_{12})(2)
H	H	L	VCS2–VCS1 (VCS_{21})(2)
H	H	H	Vss

Note 1: This is the normal state of the X3100. While in this state voltage safety conditions are periodically monitored (page 16.)

Note 2: VCS_1, VCS_2 are read at AO with respect to a DC bias voltage of 2.5V (See Section "Current Monitor Function" on page 18).

Current Monitor Function

The voltages monitored at pins VCS_1 and VCS_2 can be used to calculate current flowing through the battery terminals, using an off-board microcontroller with an A/D.

Since the value of the sense resistor (R_{SENSE}) is small (typically in the order of tens of mΩ), and since the resolution of various A/D converters may vary, the voltage across R_{SENSE} (VCS_1 and VCS_2) is amplified internally with a gain of between 10 and 160, and output to pin AO (Figure 11).

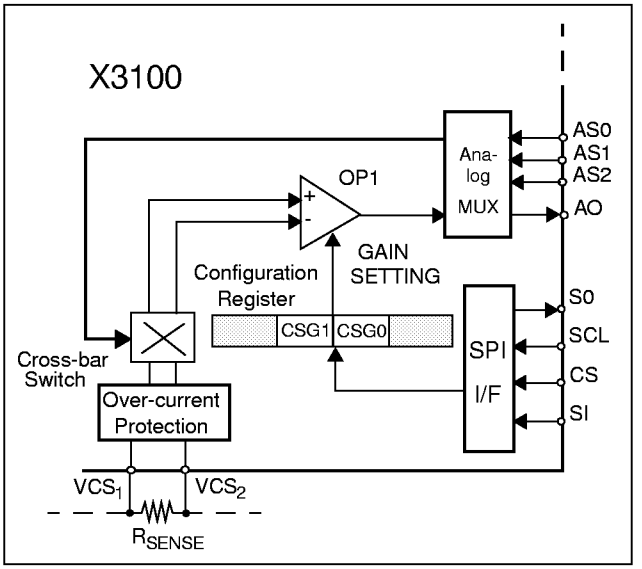


Figure 11. Current Sense Voltage Gain Setting.

The internal gain of the X3100 Current Sense voltage amplifier can be selected by issuing the WCNTR Instruction to SI, and setting bits CSG1 and CSG0 in the Control Register (Table 20).

Table 20. Current Sense Gain Control

Control Register Bits		Operation
CSG1	CSG0	
0	0	Set current sense gain=x10
0	1	Set current sense gain=x25
1	0	Set current sense gain=x80
1	1	Set current sense gain=x160

VCS1 and VCS2 are read at AO with respect to a DC bias voltage of 2.5V. Therefore, the voltage range of VCS_{12} and VCS_{21} changes depending upon the direction of current flow (i.e. battery cells are in Charge or Discharge—Table 21).

Table 21. AO Voltage Range for VCS12 and VCS21

AO	Cell State	AO Voltage Range
VCS_{12}	Charge	2.5V ≤ AO ≤ 5.0V
VCS_{12}	Discharge	0V ≤ AO ≤ 2.5V
VCS_{21}	Charge	0V ≤ AO ≤ 2.5V
VCS_{21}	Discharge	2.5V ≤ AO ≤ 5.0V

By calculating the difference of VCS_{12} and VCS_{21} the offset voltage of the internal op-amp circuitry is completely cancelled. This allows for the accurate calculation of current flow into and out of the battery cells.

Pack current is calculated using the following formula:

$$\text{Peak Current} = \frac{(VCS_{12} - VCS_{21})}{(2)(\text{gain setting})(\text{current sense resistor})}$$

CONTROL FUNCTIONS

Charge/Discharge Control

External power switching devices can be connected to pins OVP/LMON and UVP/OCP which can be used to control cell charge/discharge externally, via the SPI port.

The power switching devices should be connected such that cell discharge is possible when UVP/OCP is low (Vss), and discharge is prohibited when UVP/OCP is driven high (Vcc). The power switching devices should also be configured such that cell charge is possible when OVP/LMON is low (Vss), and cell charge is prohibited when OVP/LMON is driven high (Vcc).

UVP/OCP can be controlled by issuing the WCNTR Instruction to SI, and by setting bits OVPC and UVPC bits in the Control register (See page 5).

Table 22. UVP/OVP Control

Control Register Bits		Operation
OVPC	UVPC	
1	x	Pin OVP=Vss
0	x	Pin OVP=Vcc
x	1	Pin UVP=Vss
x	0	Pin UVP=Vcc

It is possible to set/change the values of OVPC and UVPC during a protection mode. A change in the status of the pins OVP/LMON and UVP/OCP respectively however, will not take place until the device has returned from the protection mode.

Cell Voltage Balance Control

This function can be used to adjust individual battery cell voltage during charging. Pins CB_1–CB_4 are used to control external power switching devices. Cell voltage balancing is achieved via the SPI port.

Table 23. CB1—CB4 Control

Control Register Bits				Operation
CBC4	CBC3	CBC2	CBC1	
x	x	x	1	Set CB1=Vcc
x	x	x	0	Set CB1=Vss
x	x	1	x	Set CB2=Vcc
x	x	0	x	Set CB2=Vss
x	1	x	x	Set CB3=Vcc
x	0	x	x	Set CB3=Vss
1	x	x	x	Set CB4=Vcc
0	x	x	x	Set CB4=Vss

CB1–CB4 can be controlled by issuing the WCNTR Instruction to SI, and by setting bits CBC1–CBC4 in the Control register (Table 23).

PERIODIC PROTECTION MONITORING

In normal operation, the analog select pins are set such that AS2=L, AS1=L, AS0=L. In this mode the X3100 conserves power by sampling the cells for over or under voltage conditions.

In this state over-voltage and under-voltage protection circuitry are usually off, but are periodically switched on by the internal Protection Sample Rate Timer (PSRT). The over-voltage and under-voltage protection circuitry is on for approximately 2ms in each 125ms period. Over current monitoring is continuous. In Monitor Mode (see page 18) over voltage and under voltage monitoring is also continuous.

SLEEP MODE

The X3100 can enter Sleep mode in two cases:

i) The device enters the under-voltage protection mode.

ii) The user sends the device into Sleep mode using the Control Register.

A Sleep mode can be induced by the user, by setting the SLP bit in the Control Register (Table 25). The WCNTR Instruction must be first written on SI, before the SLP bit and the remaining two bytes of the Control Register are written to the X3100.

Table 24. Sleep mode selection

Control Register Bits	
SLP	Operation
0	Normal Operation mode
1	X3100 enters Sleep mode

In Sleep mode, power to all internal circuitry is switched off hence minimizing the current drawn by the device to 1µA (max). In this state, the Discharge FET and the Charge FET are switched OFF (OVP/LMON=Vcc and UVP/OCP=Vcc), and the 5VDC regulated output (V_{RGO}) is 0V. Control of UVP/OCP and OVP/LMON via bits UVPC and OVPC in the Control Register, is also prohibited.

The device returns from Sleep mode when Vcc ≥ V_{SLR}. (e.g. when the battery terminals are connected to a battery charger). In this case, the 5VDC regulated output is restored (Section "Voltage Regulator Control" on page 21), and communication with the X3100 via the SPI port can resume.

When Vcc rises above V_{SLR}, the X3100 internally verifies that the individual Battery Cell Voltages (V_{CELL}) are larger than the Cell Charge Enable Voltage (V_{CE}). The value of VCE can be selected by first issuing the WCFIG Instruction on SI, and setting bits (Table 26) VCE1–VCE0 (and the remaining two bytes) of the Configuration Register.

Table 25. Cell Charging Threshold Voltage Selection.

Configuration Register Bits		
VCE1	VCE0	Operation
0	0	VCE=0.5V
0	1	VCE=0.80V
1	0	VCE=1.10V
1	1	VCE=1.40V

Only if the condition $V_{CELL} > V_{CE}$ is satisfied can the state of UVP/OCP and OVP/LMON be changed via the Control Register. Otherwise, if $V_{CELL} < V_{CE}$ for any battery cell then OVP/LMON and UVP/OCP are set such that both the Charge FET and the Discharge FET are OFF (OVP/LMON=Vcc and UVP/OCP=Vcc). Thus both Charge and Discharge of the battery cells via terminals P+ / P- is prohibited[1].

The cell charging threshold function can be switched ON or OFF by the user, by setting bit SWCEN in the Configuration Register (Table 27). The WCFIG Instruction must first be issued on SI, followed by the 16 bits of the Configuration Register. In the case that this cell Charge Enable function is switched OFF, then V_{CE} is effectively set to 0V, and hence will allow UVP/OVP to be switched (either automatically by the device, or via the Control Register) regardless of the value of V_{CELL}.

The X3100 cannot enter Sleep mode (neither automatically, nor by setting the Control Register) if Vcc ≥ V_{SLR}. This is to ensure that the device does not go into a Sleep mode while the battery cells are at a high voltage (e.g. during cell charging).

Table 26. Cell Charge Enable Function[1]

Configuration Register Bit	
SWCEN	Operation
0	Charge Enable function: ON
1	Charge Enable function: OFF

CELL NUMBER SELECTION

The X3100 is designed to operate with either three (3) or four (4) Li-Ion battery cells. The number of cells used, can be set by the CELLN bit of the Configuration Register (Table 28).

Table 27. Selection of number of battery cells[2]

Configuration Register Bit	
CELLN	Operation
1	4 Li-Ion battery Cells used
0	3 Li-Ion battery Cells used

The WCFIG Instruction must be first written on SI, before the CELLN bit and the remaining two bytes of the Configuration Register are written to the X3100.

VOLTAGE REGULATOR CONTROL

The X3100 is able to supply peripheral devices with a Regulated 5VDC±0.5% output at pin RGO. The Voltage regulator should be configured externally as shown in Figure 13.

The non-inverting input of OP1 is fed with a high precision 5VDC supply. The voltage at the output of the voltage regulator (V_{RGO}) is compared to this 5V reference via the inverting input of OP1. The output of OP1 in turn drives the regulator pnp transistor (Q1). The negative feedback at the regulator output maintains the voltage at 5VDC±0.5% (including ripple) despite changes in load, and differences in regulator transistors.

When power is applied to pin Vcc of the X3100, V_{RGO} is regulated to 5VDC±10% for a nominal time of T_{OC}+2ms. During this time period, V_{RGO} is "tuned" to attain a final value of 5VDC±0.5% (Figure 4, Figure 5).

The maximum current that can flow from the voltage regulator (I_{LMT}) is controlled by the current limiting resistor (R_{LMT}) connected between RGP and Vcc. When the voltage across Vcc and RGP reaches a nominal 2.5V (i.e. the threshold voltage for the FET), Q2 switches ON, shorting Vcc to the Base of Q1. Since the Base voltage of Q1 is now higher than the Emitter voltage, Q1 switches OFF, and hence V_{RGO}=0V.

Typical values for R_{LMT} and I_{LMT} are shown in Table 29. In order to protect the voltage regulator circuitry from damage in case of a short circuit, $R_{LMT} \geq 10\Omega$ should always be used.

Table 28. Typical values for R_{LMT} and I_{LMT}

R_{LMT}	Voltage Regulator Current Limit (I_{LMT})
10Ω	250mA ± 50% (Typical)
25Ω	100mA ± 50% (Typical)

When choosing the value of R_{LMT}, the drive limitations of the pnp transistor used should also be taken into consideration.

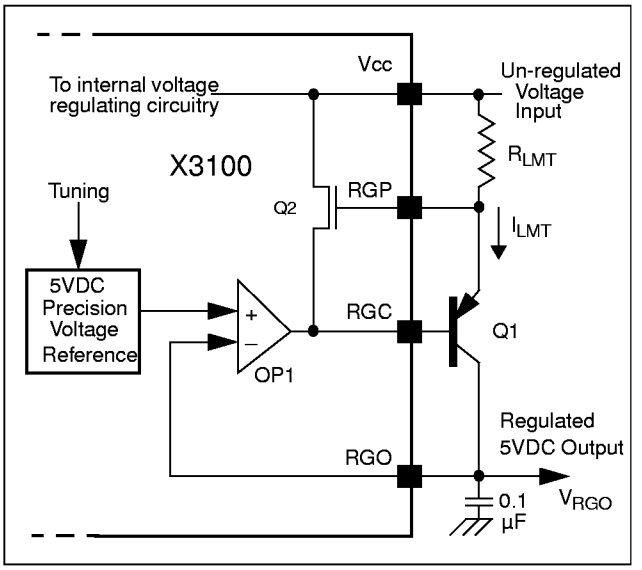


Figure 12. Voltage Regulator Operation.

1. In this case, Charging of the battery may resume ONLY if the Cell Charge Enable Function is switched OFF by setting bit SWCEN = 1 in the Configuration Register (See Above, "Configuration Register" on page 4
2. In the case that the X3100 is configured for use with only three Li-Ion Battery cells (i.e. CELLN=0), then VCELL4 (pin 7) MUST be tied to Vss (pin 9) to ensure correct operation.

4KBIT EEPROM MEMORY

The X3100 contains a CMOS 4k-bit serial EEPROM, internally organized as 512 x 8 bits. This memory is also accessible via the SPI port, and features the IDLock function.

The 4kbit EEPROM array can be accessed by the SPI port at any time, even during a protection mode, except during Sleep mode. After power is applied to Vcc of the X3100, a EEREAD and EEWRITE Instructions can be executed after times t_{PUR} (Power up to Read time) and t_{PUW} (Power up to Write time) respectively.

IDLock is a programmable locking mechanism which allows the user to lock data in different portions of the EEPROM memory space, ranging from as little as one page to as much as 1/2 of the total array. This is useful for storing information such as battery pack serial number, manufacturing codes, battery cell chemistry data, or cell characteristics.

EEPROM Write Enable Latch

The X3100 contains an EEPROM "Write Enable" latch. This latch must be SET before a write to EEPROM operation is initiated. The WREN instruction will set the latch and the WRDI instruction will reset the latch (Figure 17). This latch is automatically reset upon a power-up condition and after the completion of a byte or page write cycle.

IDLock Memory

Xicor's IDLock Memory provides a flexible mechanism to store and lock battery cell/pack information. There are seven distinct IDLock Memory areas within the array which vary in size from one page to as much as half of the entire array.

Prior to any attempt to perform an IDLock Operation, the WREN instruction must first be issued. This instruction sets the "Write Enable" latch and allows the part to respond to an IDLock sequence (Figure 18). The EEPROM memory may then be IDLocked by writing the SET IDL instruction to the device (Table 1), followed by the IDLock Protection Bytes which sets the particular partition to be locked (Table 30) as described in Figure 18.

Table 29. IDLock Partition Byte Definition

IDLock Protection Bytes	EEPROM Memory Address IDLocked
0000 0000	None
0000 0001	000h–07Fh
0000 0010	080h–0FFh
0000 0011	100h–17Fh
0000 0100	180h–1FFh
0000 0101	000h–0FFh
0000 0110	000h–00Fh
0000 0111	1F0h–1FFh

The IDLock instruction follows and consists of one command byte followed by one IDLock byte (Figure 18). This byte contains the IDLock bits IDL2-IDL0. The rest of the bits [7:3] are unused and must be written as zeroes. Bringing $\overline{CS}$ HIGH after the two byte IDLock instruction initiates a nonvolatile write to the Status Register. Writing more than one byte to the Status Register will overwrite the previously written IDLock byte.

Once an IDLock instruction has been completed, that IDLock setup is held in a nonvolatile IDLock Register (Table 31) until the next IDLock instruction is issued. The sections of the memory array that are IDLocked can be read but not written until IDLock is removed or changed.

Table 30. IDLock Register

7	6	5	4	3	2	1	0
0	0	0	0	0	IDL2	IDL1	IDL0

Note: Bits [7:3] specified to be "0's"

EEPROM Read Sequence (EEREAD)

When reading from the X3100 EEPROM memory, $\overline{CS}$ is first pulled LOW to select the device. The 8-bit EEREAD instruction is transmitted to the X3100, followed by the 16-bit address, of which the last 9 bits are used (bits [15:9] specified to be zeroes). After the EEREAD opcode and address are sent, the data stored in the memory at the selected address is shifted out on the SO line. The data stored in memory at the next address can be read sequentially by continuing to provide clock pulses. The address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached (01FFh), the address counter rolls over to address 0000h, allowing the read cycle to be continued indefinitely. The read

operation is terminated by taking $\overline{CS}$ HIGH. Refer to the EEPROM Read (EEREAD) Operation Sequence illustrated in Figure 19.

EEPROM Read Status Operation (EEREAD STAT)

If there is not a nonvolatile write in progress, the EEREAD STAT instruction returns the ID Lock byte from the IDLock Register which contains the ID Lock bits IDL2-IDL0 (Table 30). The ID Lock bits define the ID Lock condition (Table 30/Table 31). The other bits are reserved and will return '0' when read. See Figure 20.

If a nonvolatile write to the EEPROM (i.e. EEWRITE Instruction) is in progress, the EEREAD STAT returns a HIGH on SO. When the nonvolatile write cycle in the EEPROM is completed, the status register data is read out.

Clocking SCK is valid during a nonvolatile write in progress, but is not necessary. If the SCK line is clocked, the pointer to the status register is also clocked, even though the SO pin shows the status of the nonvolatile write operation (See Figure 20).

EEPROM Write Sequence (EEWRITE)

Prior to any attempt to write data into the EEPROM of the X3100, the "Write Enable" latch must first be set by issuing the WREN instruction (See Table 1 and Figure 17). $\overline{CS}$ is first taken LOW. Then the WREN instruction is clocked into the X3100. After all eight bits of the instruction are transmitted, $\overline{CS}$ must then be taken HIGH. If the user continues the write operation without taking $\overline{CS}$ HIGH after issuing the WREN instruction, the write operation will be ignored.

To write data to the E2PROM memory array, the user then issues the EEWRITE instruction, followed by the 16 bit address and the data to be written. Only the last 9 bits of the address are used and bits [15:9] are specified to be zeroes. This is minimally a thirty-two clock operation. $\overline{CS}$ must go LOW and remain LOW for the duration of the operation. The host may continue to write up to 16 bytes of data to the X3100. The only restriction is the 16 bytes must reside on the same page. If the address counter reaches the end of the page and the clock continues, the counter will "roll over" to the first address of the page and overwrite any data that may have been previously written.

For a byte or page write operation to be completed, $\overline{CS}$ can only be brought HIGH after bit 0 of the last data byte to be written is clocked in. If it is brought HIGH at any other time, the write operation will not be completed. Refer to Figures 21 and 22 for detailed illustration of the write sequences and time frames in which $\overline{CS}$ going HIGH are valid.

TYPICAL APPLICATION CIRCUIT

The X3100 has been designed to operate correctly when used as connected in the Typical Application Circuit (Figure 1).

The power MOSFET's Q1 and Q2 are referred to as the "Discharge FET" and "Charge FET" respectively. Since these FETs are p-channel devices, they will be ON when UVP/OVP is at level Vss, and OFF when UVP/OVP is at level Vcc. As their name implies, the Discharge FET is used to control cell discharge, while the Charge FET is used to control cell charge. Diode D1 allows the battery cells to receive charge even if the Discharge FET is OFF, while diode D2 allows the cells to discharge even if the Charge FET is OFF. It should be noted that the cells can neither charge nor discharge if both the Charge FET and Discharge FET are OFF.

Power to the X3100 is applied to pin Vcc, via diodes D6 and D7. These diodes allow the device to be powered by the Li-Ion battery cells in normal operating conditions, while being powered by an external source via pin P+ when the battery cells are being charged. These diodes should have sufficient current and voltage ratings to handle both cases of battery cell charge and discharge.

The operation of the voltage regulator is described in Section "VOLTAGE REGULATOR CONTROL" on page 21, and provides a 5VDC±0.5% output—V_{RGO} (including ripple). The bypass capacitor C_{PS} connected from RGO to ground should be included to improve (reduce) ripple voltage. At typical value for C_{PS} is 0.1µF.

Before the nominal time (T_{OC} + 2ms), V_{RGO} has an output in the range of 5VDC ± 10% (Figure 4, Figure 5). Depending upon the type of microcontroller used, this voltage may not be sufficient to operate correctly. Therefore, the designer may choose to wait (T_{OC} + 2ms) before attempting to perform any read operation on the X3100, even though such an instruction can be correctly handled by the device after time t_{PUR}.

V_{RGO} can be also used as a reference voltage for a battery pack temperature sensor. Figure 1 shows the temperature sensor implemented as a simple resistive voltage divider, utilizing a Thermistor (R_T) and resistor (R'_T). The voltage V_T can be fed to the A/D input of a

microcontroller, and used to measure and monitor the temperature of the battery cells. R'_T should be chosen with consideration of the dynamic resistance range of R_T, as well as the input voltage range of the microcontroller A/D input. V_{RGO} is also used as a reference voltage for the A/D input of the microcontroller.

Diode D3 is included to facilitate Load Monitoring in an Over-current protection mode (Section "Over-Current Protection" on page 16), while preventing the flow of current into pin OVP/LMON during normal operation.

Resistor R_{PU} is connected across the Gate and Drain of the Charge FET (Q2). Q1 is turned off by the X3100, and hence the voltage at pin OVP/LMON will be (at maximum) the voltage of the battery terminal, minus one forward biased diode voltage drop (V_{P+}–V_{D7}). Since the Drain of Q2 is connected to a higher potential, a pull-up resistor (R_{PU}) in the order of 1MΩ should be used to ensure that the Charge FET is completely turned OFF when OVP/LMON=Vcc.

The capacitors C_{LPF}, and resistors R_{LPF}, are used in a first order low pass filter configuration, at the Battery Cell Voltage monitoring inputs (VCELL1–VCELL4) of the X3100. This circuit is used to block any unwanted interference signals from being inadvertently injected into the monitor inputs. These interference signals may result from:

- Transients created at battery contacts when the battery pack is being connected/disconnected from the charger or the host.
- Electrostatic discharge (ESD) from something/someone touching the battery contacts.
- Unfiltered noise that exists in the host device.
- RF signals which are induced into the battery pack from the surrounding environment.

Such interference can cause the X3100 to operate in an unpredictable manner, or in extreme cases, damage the device. As a guide, C_{LPF} should be in the order of 0.1µF and R_{LPF}, should be in the order of 1kΩ. Capacitors C_{LPF} should be of the ceramic type. In order to minimize interference, PCB tracks should be made as short and as wide as possible to reduce their impedance. The battery cells should also be placed as close to the X3100 monitor inputs as possible.

Resistors R_{CB} and the associated n-channel MOSFET's (Q_6–Q_9) are used for battery Cell voltage Balancing. The X3100 provides internal drive circuitry which allows the user to switch FETs Q_6–Q_9 ON or OFF via the microcontroller and SPI port (Section "Cell Voltage Balance Control" on page 19). When any of the these FETs are switched ON, a current, limited by resistor R_{CB}, flows across the particular battery cell. In doing so, the user can control the voltage across each individual battery cell. This is important when using Li-Ion battery cells since imbalances in cell voltages can, in time, greatly reduce the useable capacity of the battery pack. Cell voltage balancing may be implemented in various ways, but is usually performed towards the end of cell charging (“Top-of-charge method”). Values for R_{CB} will vary according to the specific application.

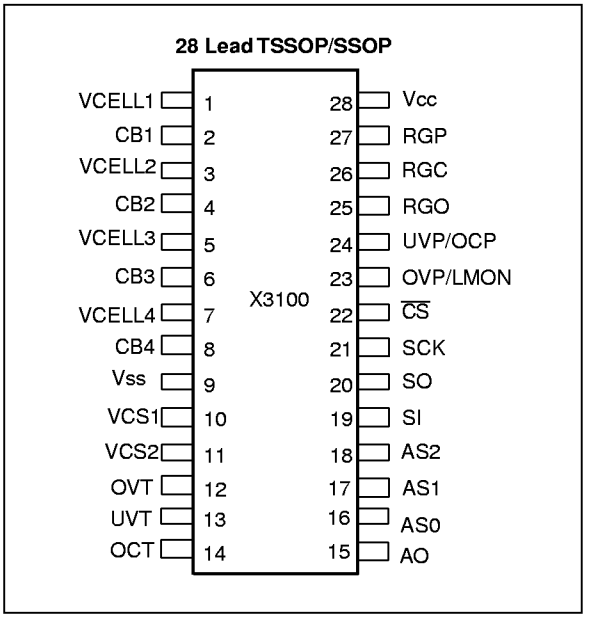
The internal 4kbit EEPROM memory can be used to store the cell characteristics for implementing such functions as gas gauging, battery pack history, charge/discharge cycles, and minimum/maximum conditions. Battery pack manufacturing data as well as serial number information can also be stored in the EEPROM array.

A current sense resistor (R_{SENSE}) is used to measure and monitor the current flowing into/out of the battery terminals, and is used to protect the pack from Over-current conditions (Section "Over-Current Protection" on page 16). R_{SENSE} is also used to externally monitor current via a microcontroller (Section "Current Monitor Function" on page 18). It should be noted that when externally monitoring the voltage across this sense resistor, some degree of non-linearity may be introduced at the analog output (AO) due to the internal op-amp (Figure 11). This non-linearity can be corrected by storing the op-amp characteristics in the EEPROM array, and making the appropriate compensation when calculating current flow in the micro-controller.

PIN NAMES

Pin	Symbol	Description
1	VCELL1	Battery cell voltage 1
2	CB1	Cell Balancing FET control output 1
3	VCELL2	Battery cell vdoltage 2
4	CB2	Cell Balancing FET control output 2
5	VCELL3	Battery cell voltage 3
6	CB3	Cell Balancing FET control output 3
7	VCELL4	Battery cell voltage 4
8	CB4	Cell Balancing FET control output 4
9	Vss	Ground
10	VCS1	Current Sense voltage pin 1
11	VCS2	Current Sense voltage pin 2
12	OVT	Over-voltage detection/release time control
13	UVT	Under-voltage detection/release time control
14	OCT	Over-current detection/release time control
15	AO	Analog multiplexer output
16	AS0	Analog output select pin 0
17	AS1	Analog output select pin 1
18	AS2	Analog output select pin 2
19	SI	Serial Data Input
20	SO	Serial Data Output
21	SCK	Serial Data Clock
22	$\overline{CS}$	Chip Select pin
23	OVP/LMON	Over-voltage protection control/Load Monitor function
24	UVP/OCP	Under-voltage protection control/ Over-current protection control
25	RGO	Voltage regulator Output pin
26	RGC	Voltage regulator Control pin
27	RGP	Voltage regulator Protection pin
28	Vcc	Power supply (from Battery terminals)

PIN CONFIGURATION



PIN DESCRIPTIONS

Battery cell voltage (VCELL1-VCELL4): Pins 1,3,5,7

These pins are used to monitor the voltage of each battery cell internally. The voltage of an individual cell can also be monitored externally at pin AO.

The X3100 is designed to monitor 3 or 4 battery cells. In the case that only 3 cells are used, pin VCELL4 must be tied to ground (Vss).

Cell Voltage Balancing Control (CB1-CB4): Pins 2,4,6,8

These outputs are used to switch external FETs in order to perform cell voltage balancing control. This function can be used to adjust individual cell voltages (e.g. during cell charging). CB1–CB4 can be driven high (Vcc) or low (Vss) to switch external FETs ON/OFF.

Current Sense Inputs (VCS1–VCS2): Pins 10,11

A sense resistor (R_{SENSE}) is connected in series between VCS1 and VCS2 (Figure 1). R_{SENSE} has a resistance in the order of mΩ, and is used to monitor current flowing through the battery terminals, and protect against over-current conditions. The voltage of at each end of R_{SENSE} can also be monitored at pin AO.

Over-voltage detection time control (OVT): Pin 12

This pin is used to control the delay time (T_{OV}) associated with the detection of an over-voltage condition (Section "Over-Voltage Protection" on page 11).

Under-voltage detection/release time control (UVT): Pin 13

This pin is used to control the delay times associated with the detection (T_{UV}) and release (T_{UVR}) of an under-voltage condition (Section "Under-Voltage Protection" on page 13).

Over-current detection/release time control (OCT): Pin 14

This pin is used to control the delay times associated with the detection (T_{OC}) and release (T_{OCR}) of an over-current condition (Section "Over-Current Protection" on page 16).

Analog output (AO): Pin 15

The analog output pin is used to externally monitor various battery parameter voltages. The voltages which can be monitored at AO (Section "Analog Multiplexer Selection" on page 18) are:

- Individual cell voltages
- Voltage across the current sense resistor (R_{SENSE}). This voltage is amplified with a gain set by the user in the Control Register (Section "Current Monitor Function" on page 18.)

The desired voltage to be monitored can be selected to AO by using pins AS0–AS2.

Analog output select (AS0–AS2): Pins 16,17

These pins are used to select which voltage is to be multiplexed to the output AO (See Section "Charge/Discharge Control" on page 19 and Section "Current Monitor Function" on page 18)

Serial Input (SI): Pin 19

SI is the serial data input pin. All opcodes, byte addresses, and data to be written to the device are input on this pin. Data is latched by the rising edge of the serial clock.

Serial Output (SO):
Pin (20)

SO is a push/pull serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock. While $\overline{CS}$ is HIGH, then SO will be in the High Impedance state.

Note: SI and SO may be tied together to form one line (SI/SO). In this case, all serial data communication with the X3100 is undertaken over one I/O line. This is permitted ONLY if no simultaneous read/write operations occur.

Serial Clock (SCK):
Pin 21

The Serial Clock controls the serial bus timing for data input and output. Opcodes, addresses, or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin change after the falling edge of the clock input.

Chip Select ($\overline{CS}$):
Pin 22

When $\overline{CS}$ is HIGH, the device is deselected and the SO output pin is at high impedance. $\overline{CS}$ LOW enables the SPI serial bus.

OVP/LMON:
Pin 23

This one pin performs two functions depending upon the present mode of operation of the X3100.

- **Over-voltage protection (OVP)**

In Normal Operation Mode, this pin (OVP/LMON) is used to control the switching of battery cell charge. OVP/LMON drives an external power FET which should be configured such that cell charge is possible when OVP/LMON=Vss, and cell charge is prohibited when OVP/LMON=Vcc. Such a configuration prevents damage of the battery cells due to the application of high voltage for an extended period of time (Section "Over-Voltage Protection" on page 11).

- **Load Monitor (LMON)**

In Over-current Protection mode, a small test current (7.5µA typ.) is passed out of this pin (OVP/LMON) to sense the load resistance. The measured load resistance determines whether or not the X3100 returns from an Over-current protection mode (Section "Over-Current Protection" on page 16).

Under Voltage Protection / Over Current Protection (UVP/OCP) : Pin 24

Pin UVP/OCP is used to control the switching of battery cell discharge via an external power FET. This FET should be configured such that cell discharge is possible when UVP/OCP=Vss, and cell discharge is prohibited when UVP/OCP=Vcc. The UVP/OCP pin is switched when the X3100 enters either:

- Under-voltage protection mode (Section "Under-Voltage Protection" on page 13)

In this case, pin 24 is referred to as “Under-voltage protection (UVP)”. UVP/OCP is switched to prevent the battery cells from being damaged by being exposed to excessively low voltages.

- Over-current protection mode (Section "Over-Current Protection" on page 16)

In this case, pin 24 is referred to as “Over-current protection (OCP)”. UVP/OCP is switched to prevent damage to the battery cells caused by excessive current drain (e.g. as in the case of a short circuit of the battery terminals).

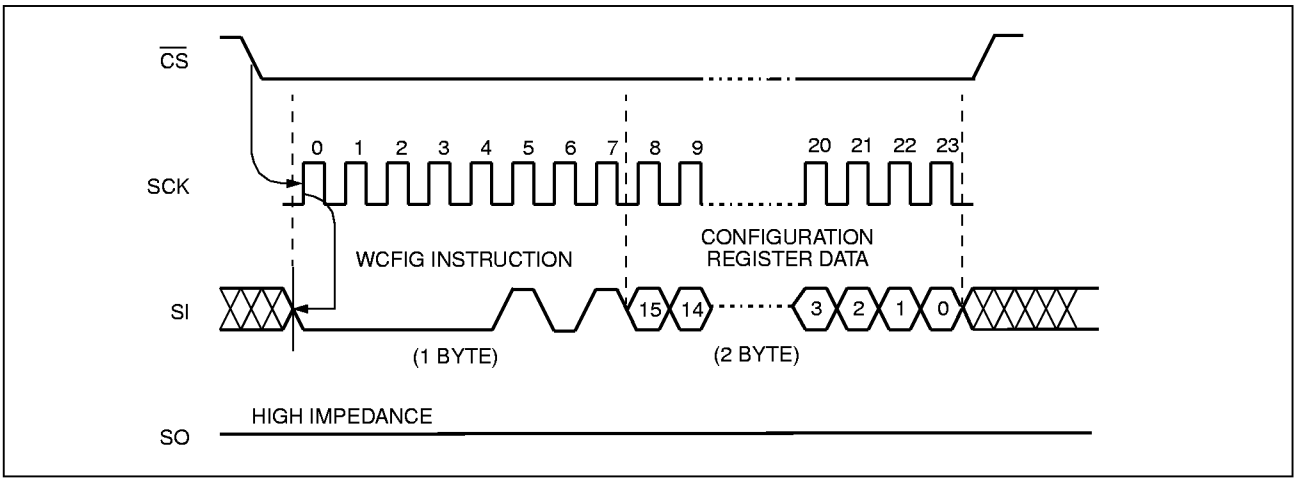


Figure 13. Write Configuration Register (WCFIG) Operation Sequence

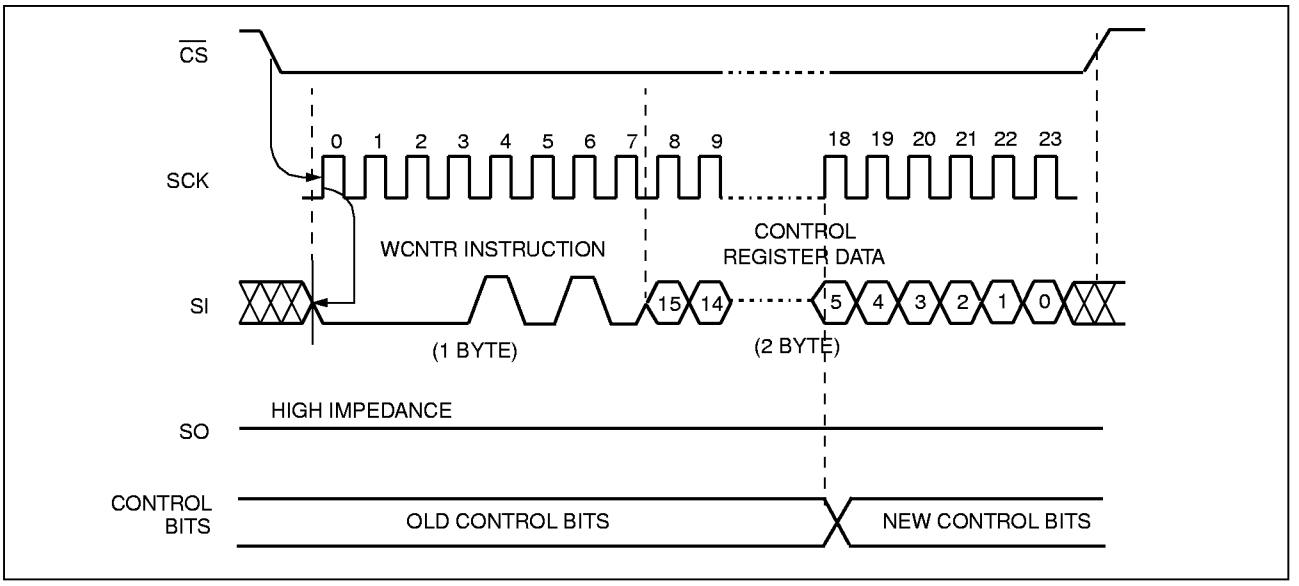


Figure 14. Write Control Register (WCNTR) Operation Sequence

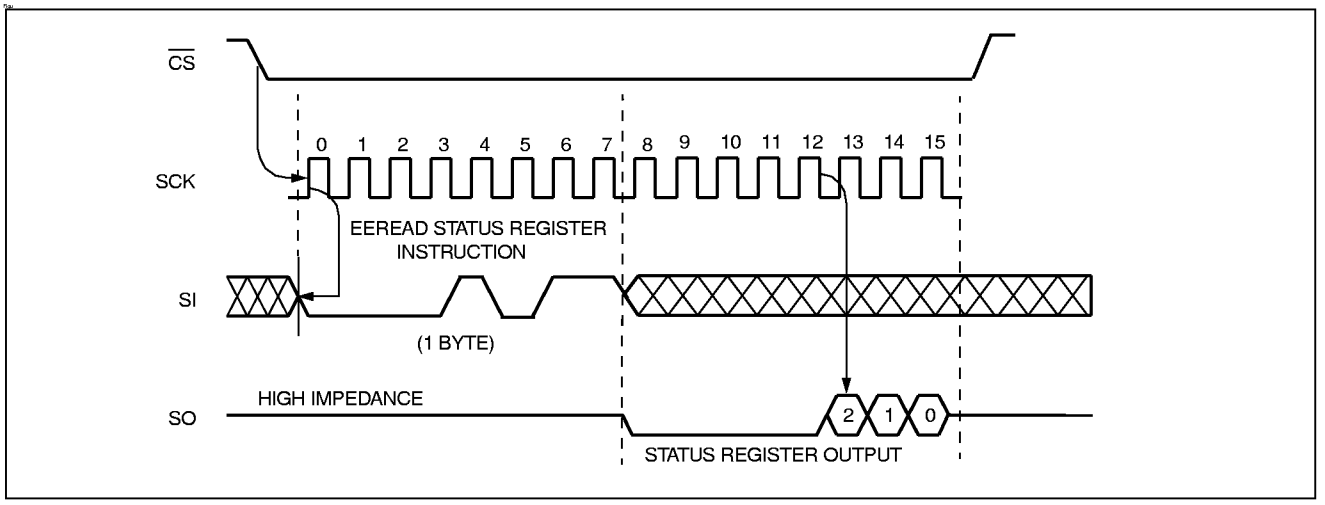


Figure 15. Read Status Register (RDSTAT) Operation Sequence

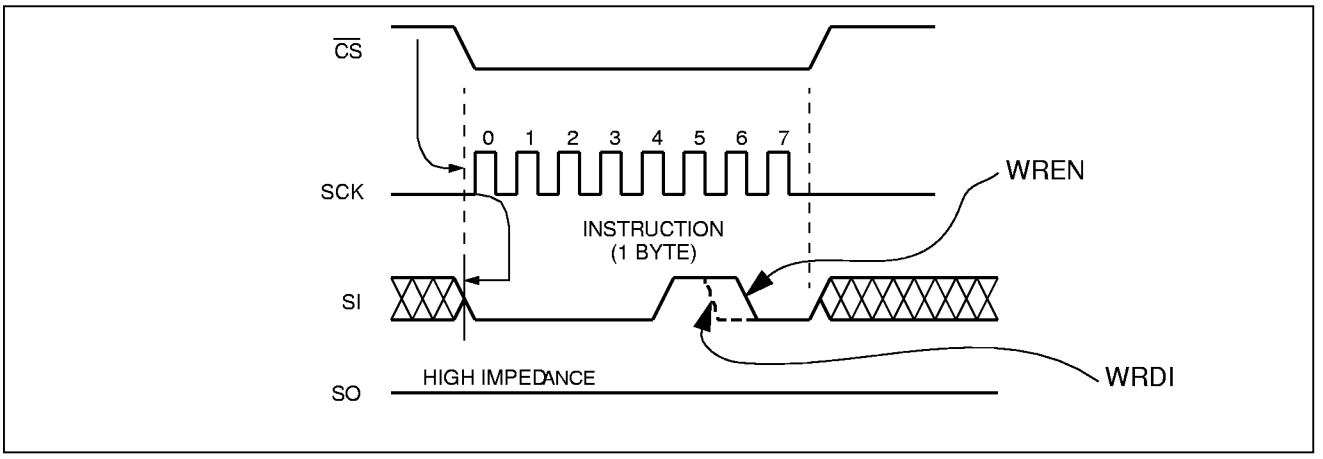


Figure 16. EEPROM Write Enable Latch (WREN/WRDI) Operation Sequence

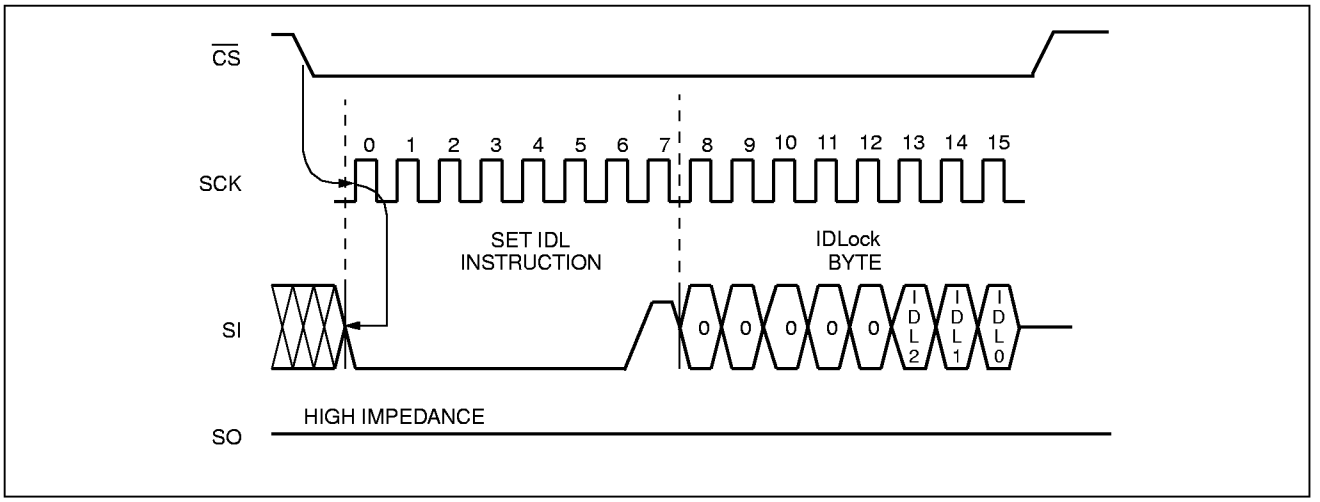


Figure 17. EEPROM IDLock (SET IDL) Operation Sequence

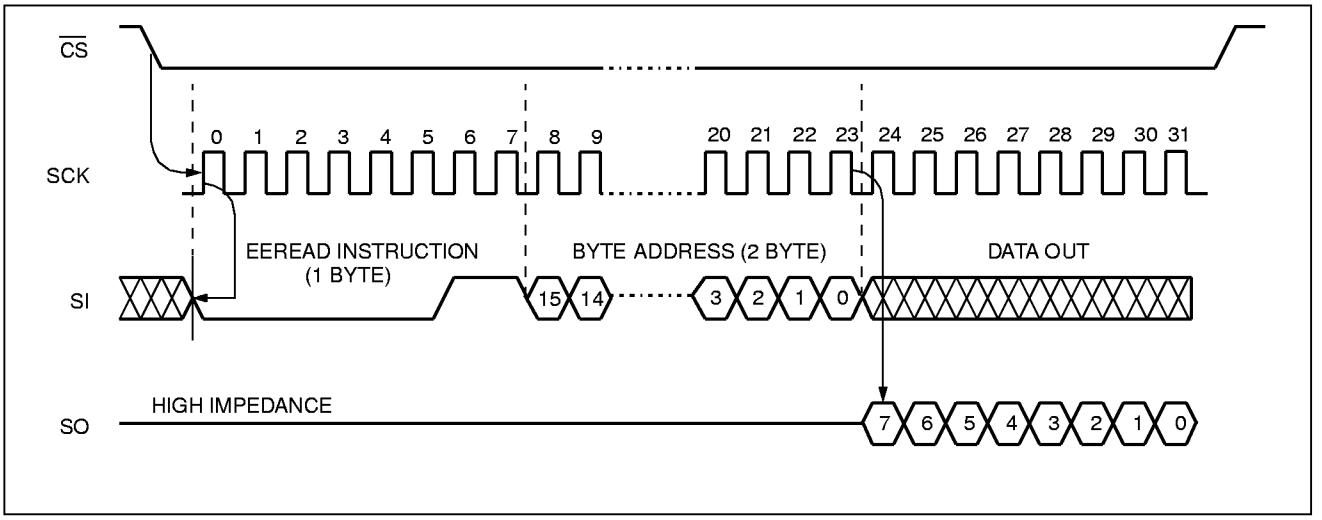

CS
SCK
0 1 2 3 4 5 6 7 8 9 20 21 22 23 24 25 26 27 28 29 30 31
EEREAD INSTRUCTION
(1 BYTE)
BYTE ADDRESS (2 BYTE)
DATA OUT
SI
15 14 3 2 1 0
HIGH IMPEDANCE
SO
7 6 5 4 3 2 1 0

Figure 18. EEPROM (EEREAD) Read Operation Sequence

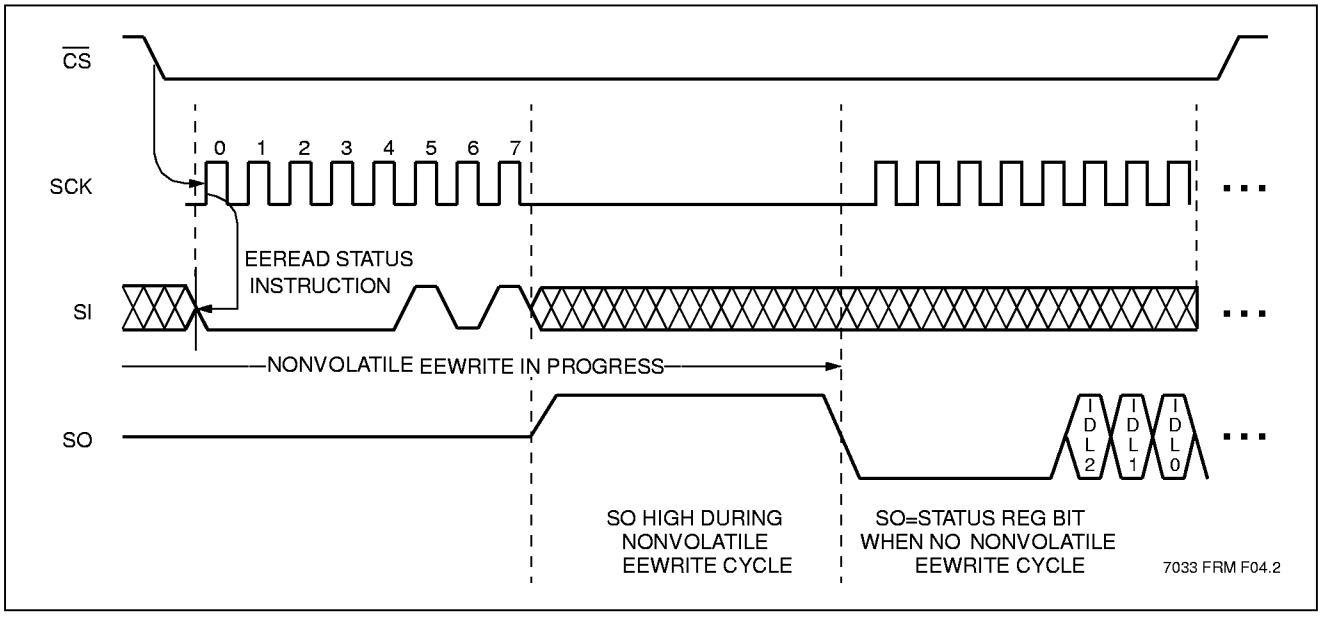


Figure 19. EEPROM Read Status (EEREAD STAT) Operation Sequence

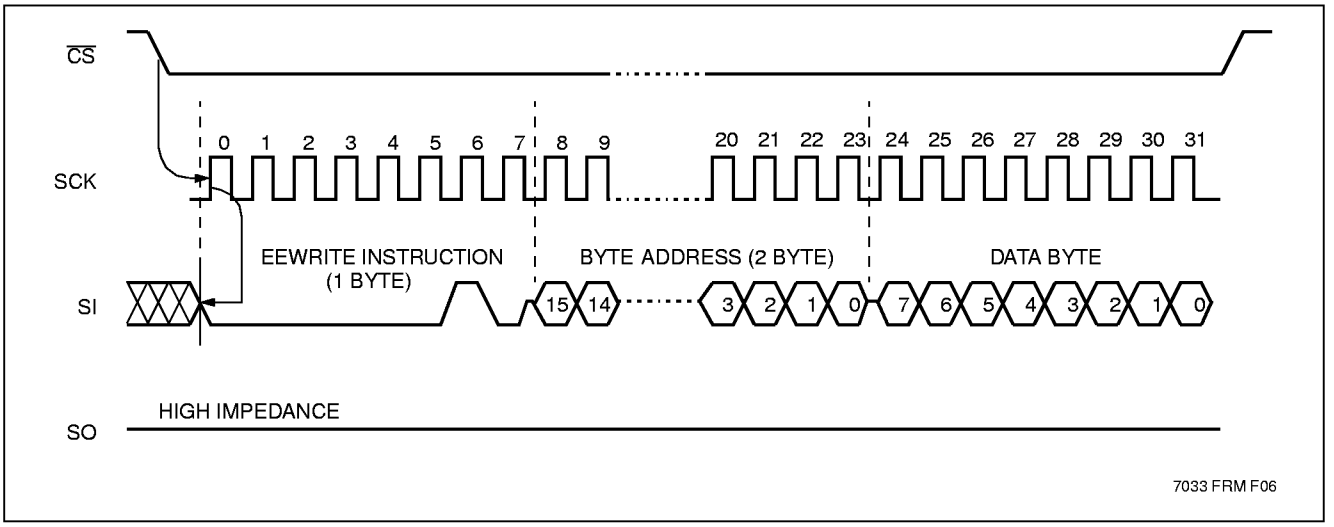


Figure 20. EEPROM Byte Write (EEWRITE)Operation Sequence

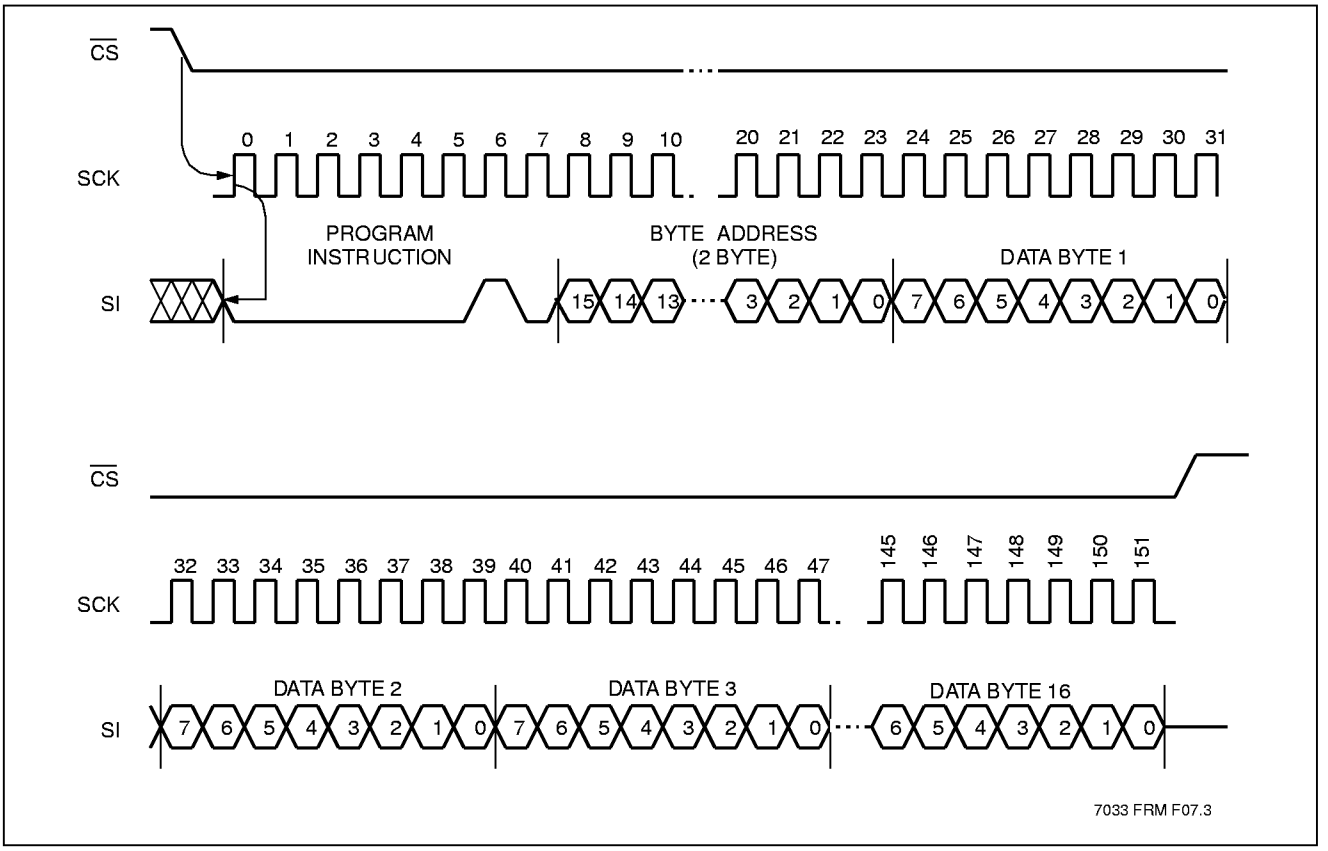


Figure 21. EEPROM Page Write (EEWRITE) Operation Sequence

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min.	Max.	Unit
	Storage Temperature	-55	125	°C
	Operating Temperature	-40	85	°C
	DC Output Current		5	mA
	Lead Temperature (Soldering 10 seconds)		300	°C
Vcc	Power Supply Voltage	Vss-0.5	Vss+27.0	V
Vcell	Cell Voltage	-0.5	7.0	V
V_{TERM1}	Terminal Voltage (Pins:SCK, SI, SO, CS, AS0, AS1, AS2, VCS1, VCS2, OVT, UVT, OCT, AO)	Vss-0.5	V_{RGO} + 0.5	V
V_{TERM2}	Terminal Voltage (V_{CELL4})	Vss-0.5	Vcc + 1.0	V
V_{TERM3}	Terminal Voltage (all other pins)	Vss-0.5	Vcc + 0.5	V

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	-20°C	+70°C

Supply Voltage	Limits
X3100	6V to 24V

D.C. OPERATING CHARACTERISTICS—PINS:

(Over the recommended operating conditions, unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{LI}	Input Leakage Current		10	µA	
I_{LO}	Output Leakage Current		10	µA	
V_{IL}(1)	Input LOW Voltage (SCK, SI, SO, CS, AS0, AS1, AS2)	- 0.3	V_{RGO} x 0.3	V	
V_{IH}(1)	Input HIGH Voltage (SCK, SI, SO, CS, AS0, AS1, AS2)	V_{RGO} x 0.7	V_{RGO} + 0.3	V	
VOL1	Output LOW Voltage (SCK, SI, SO, CS, AS0, AS1, AS2)		0.4	V	I_{OL} = 1.0mA
VOH1	Output HIGH Voltage (SCK, SI, SO, CS, AS0, AS1, AS2)	V_{RGO} x 0.3		V	I_{OH} = -0.4mA
VOL2	Output LOW Voltage (UVP/OCP, OVP/LMON, CB1-CB4)		0.4	V	I_{OL} = 100uA
VOH2	Output HIGH Voltage (UVP/OCP, OVP/LMON, CB1-CB4)	Vcc-0.4		V	I_{OH} = -20uA
VOL3	Output LOW Voltage (RGC)		0.4	V	I_{OL} = 2mA
VOH3	Output HIGH Voltage (RGC)	V_{RGO}-0.1V		V	I_{OH} =-0.8mA

POWER-UP TIMING

Symbol	Parameter	Min.	Max.	Units
t_{PUR}(2)	Power-up to SPI Read Operation (RDSTAT, EEREAD STAT)		1	ms
t_{PUW}(2)	Power-up to SPI Write Operation (WREN, WRDI, EEWRITE, WCFIG, WCNTR, SET IDL)		5	ms

Notes: (1) V_{IL} Min. and V_{IH} Max. are for reference only and are not 100% tested.
(2) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until a can be initiated. These parameters are periodically sampled and not 100% tested.

OPERATING CHARACTERISTICS (Over recommended operating conditions)

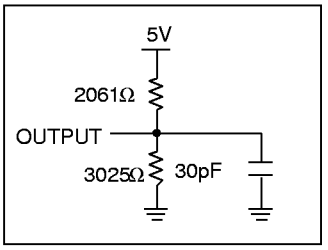
Description	Sym	Condition	Min	Typ(4)	Max	Unit
5V Regulated Voltage	V_{RGO}	On power up	4.5		5.5	V
		After automatic tuning	4.95	5.0	5.05	V
Vcc Supply Current (1)	Icc1	Normal Operation		85	250	µA
Vcc Supply Current (2)	Icc2	during non volatile EEPROM write		1.3	2.5	mA
Vcc Supply Current (3)	Icc3	During EEPROM read SCK=3.3MHz		0.9	1.2	mA
Vcc Supply Current (4)	Icc4	Sleep mode			1	µA
Vcc Supply Current (5)	Icc5	Monitor Mode AN2, AN1, AN0 not equal to 0.		365	600	µA
Cell over-voltage protection mode threshold	V_{OV}	V_{OV}=4.20V (Default)(3)		4.20	4.25	V
Cell over-voltage protection mode release threshold	V_{OVR}	V_{OV}=4.20V (Default)(3)	3.9	4.0	4.1	V
Cell over-voltage detection time	T_{OV}	C_{OV}=0.1uF	0.5	1	1.5	s
Cell under-voltage protection mode (SLEEP) threshold.	V_{UV}	V_{UV}=2.3V (Default)(3)	2.15	2.25	2.35	V
Cell under-voltage protection mode release threshold	V_{UVR}	V_{UV}=2.3V (Default)(3)	2.7	2.95	3.2	V
Cell under-voltage detection time	T_{UV}	C_{UV}=0.1µF	0.5	1	1.5	s
Cell under-voltage release time	T_{UVR}	C_{UV}=0.1µF	3.5	7	10.5	ms
Over-current mode Detection Voltage	V_{OC}	V_{OC}=0.1V (Default)(3)	0.085	0.100	0.115	V
Over-current mode Detection Time	T_{OC}	C_{OC}=1nF	5	10	15	ms
Over-current mode Release Time	T_{OCR}	C_{OC}=1nF	5	10	15	ms
Load Resistance Over-current mode Release Condition		Releases when OVP/LMON pin > 2.5V	200	250		kΩ
Cell Charge Threshold Voltage	V_{CE}	V_{CE}=1.4V (Default)(3)	1.30	1.40	1.50	V
5VDC Voltage Regulator Current Limit	I_{LMT}	R_{LMT}=10Ω		250		mA
Vcc voltage necessary to guarantee return from Sleep mode	V_{SLR}		16.0			V

Notes: (3) This value is set at the time of shipping, but may be changed by the user via settings in the internal registers
(4) Typical at 25°C

CAPACITANCE T_A=+25°C, F= 1 MHZ, V_{RGO}=5V

Symbol	Parameter	Max.	Units	Conditions
C_{OUT}(5)	Output Capacitance (SO)	8	pF	V_{OUT}=0V
C_{IN}(5)	Input Capacitance (SCK, SI, $\overline{CS}$)	6	pF	V_{IN}=0V

Equivalent A.C. Load Circuit



A.C. TEST CONDITIONS

Input Pulse Levels	0.5 – 4.5V
Input Rise and Fall Times	10ns
Input and Output Timing Level	2.5V

A.C. CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

Data Input Timing

Symbol	Parameter	Voltage	Min.	Max.	Units
f_{SCK}	Clock Frequency		0	3.3	MHz
t_{CYC}	Cycle Time		300		ns
t_{LEAD}	$\overline{CS}$ Lead Time		150		ns
t_{LAG}	$\overline{CS}$ Lag Time		150		ns
tWH	Clock HIGH Time		130		ns
tWL	Clock LOW Time		130		ns
tSU	Data Setup Time		20		ns
tH	Data Hold Time		20		ns
tRI(5)	Data In Rise Time			2	µs
tFI(5)	Data In Fall Time			2	µs
tCS	$\overline{CS}$ Deselect Time		100		ns
tWC(6)	Write Cycle Time			5	ms

7033 FRM T10

Notes: (5) This parameter is periodically sampled and not 100% tested.

(6) t_{WC} is the time from the rising edge of $\overline{CS}$ after a valid write sequence has been sent to the end of the self-timed internal nonvolatile write cycle.

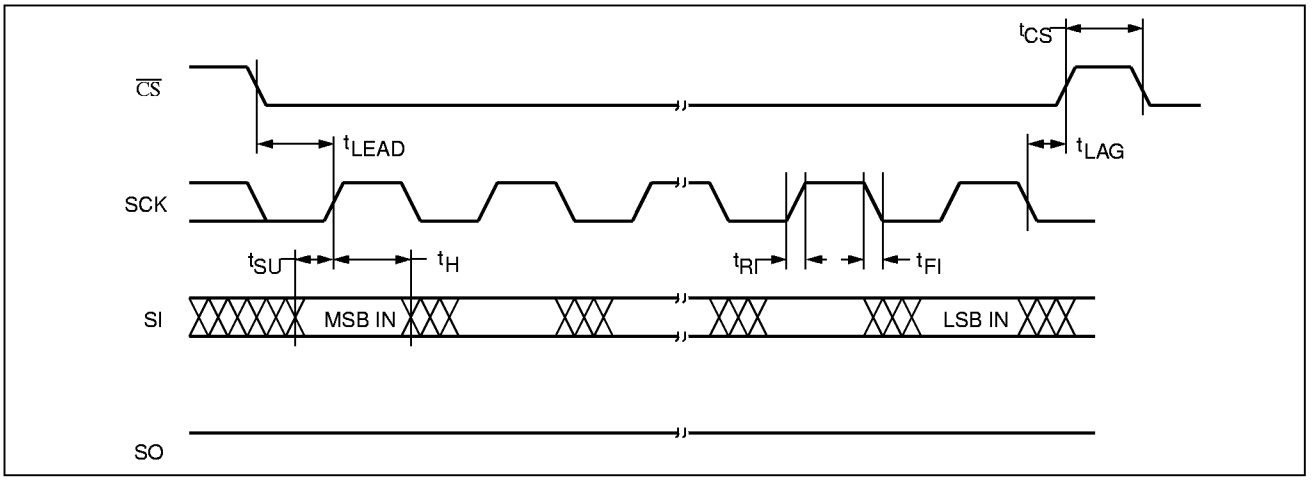


Figure 22. Serial Input Timing

Data Output Timing

Symbol	Parameter	Voltage	Min.	Max.	Units
f_{SCK}	Clock Frequency		0	3.3	MHz
t_{DIS}	Output Disable Time			150	ns
t_V	Output Valid from Clock LOW			130	ns
t_{HO}	Output Hold Time		0		ns
t_{RO}(7)	Output Rise Time			50	ns
t_{FO}(7)	Output Fall Time			50	ns

Notes: (7) This parameter is periodically sampled and not 100% tested.

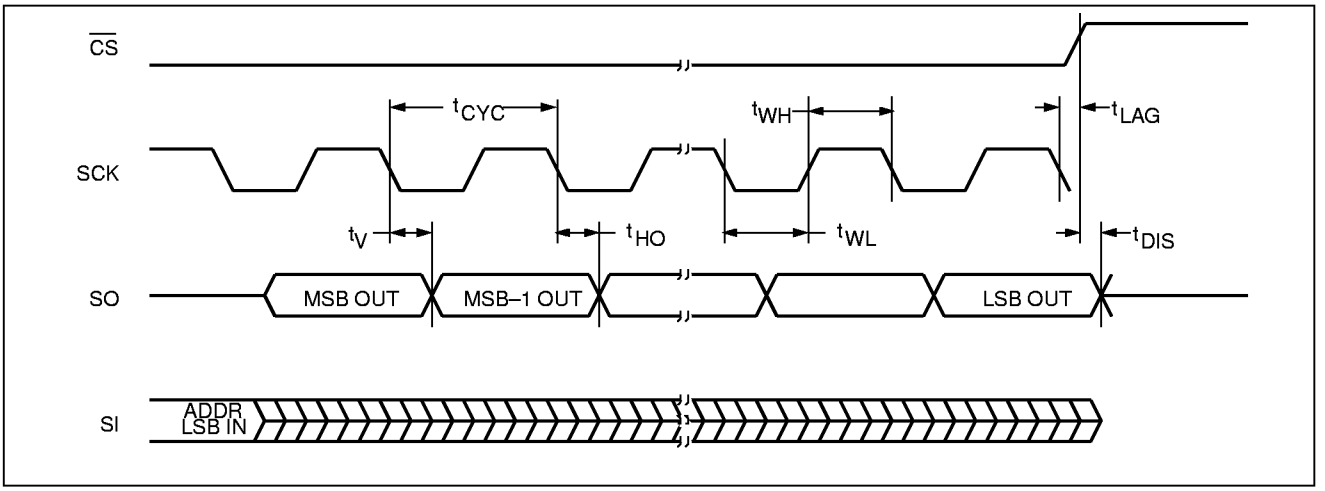
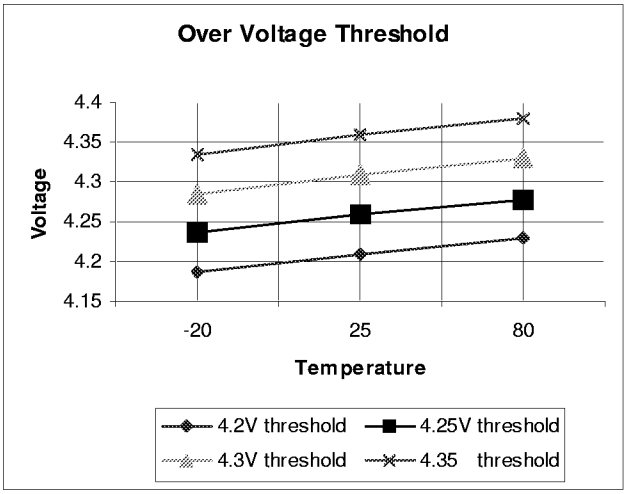


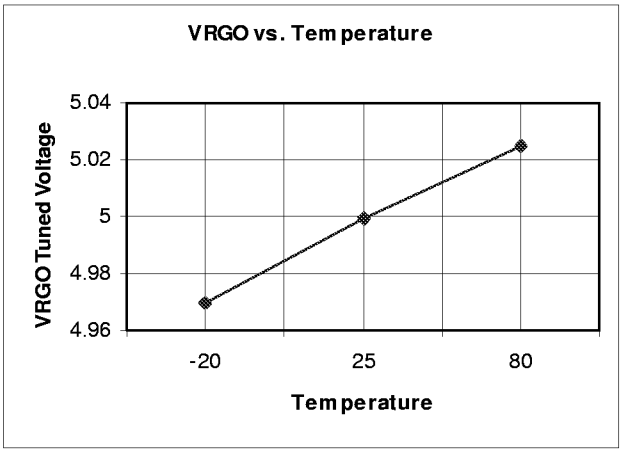
Figure 23. Serial Output Timing

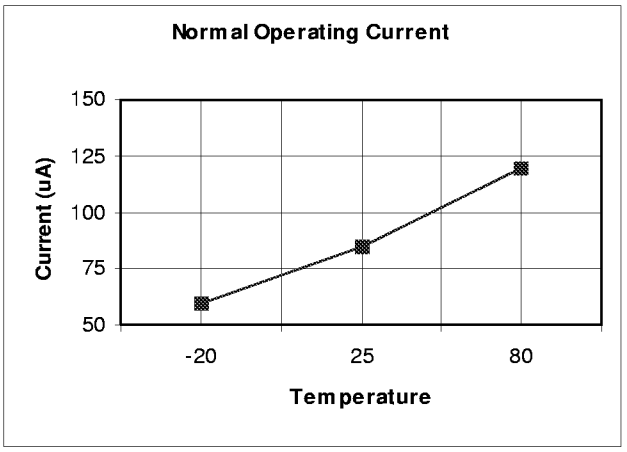
SYMBOL TABLE

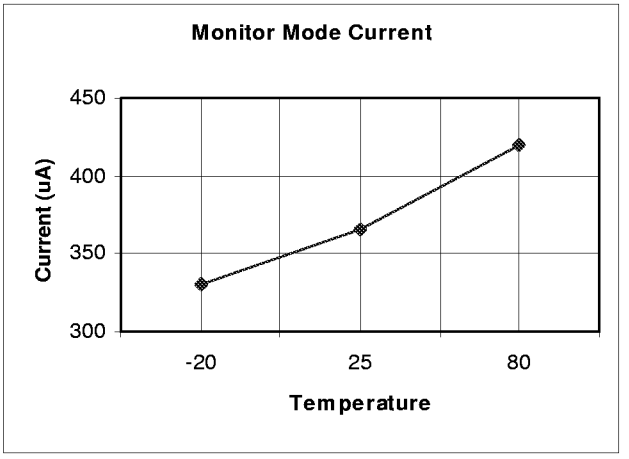
WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

OVER VOLTAGE THRESHOLD

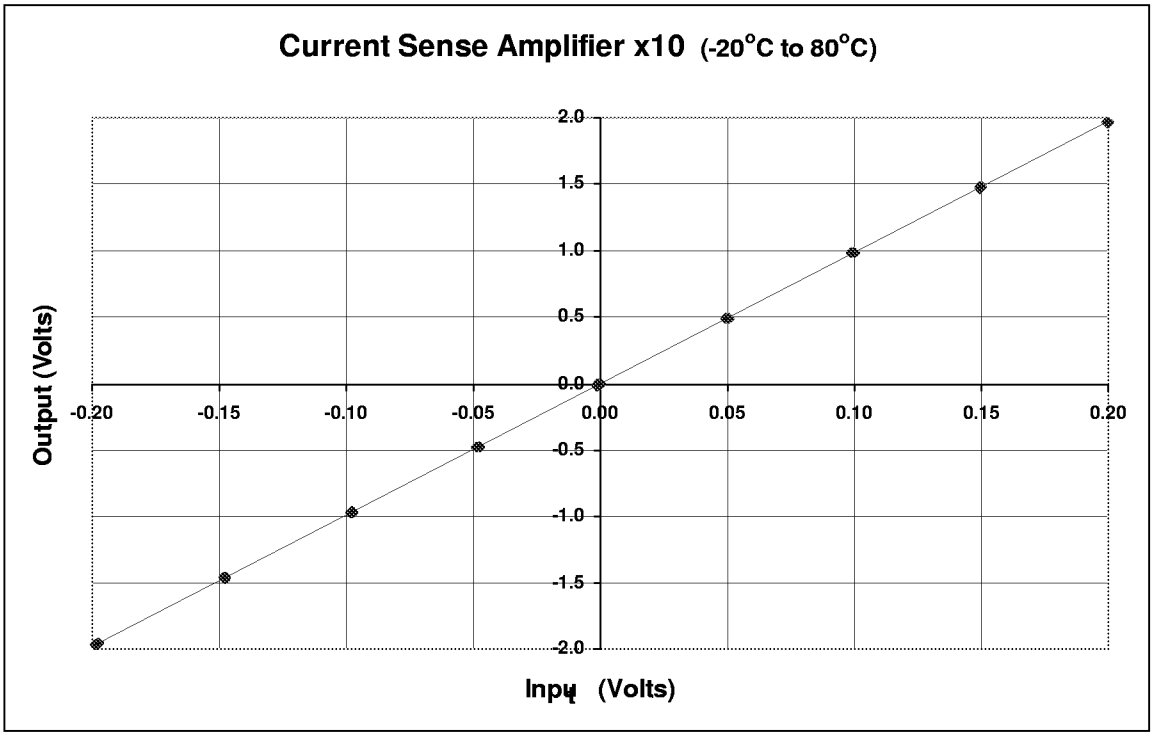


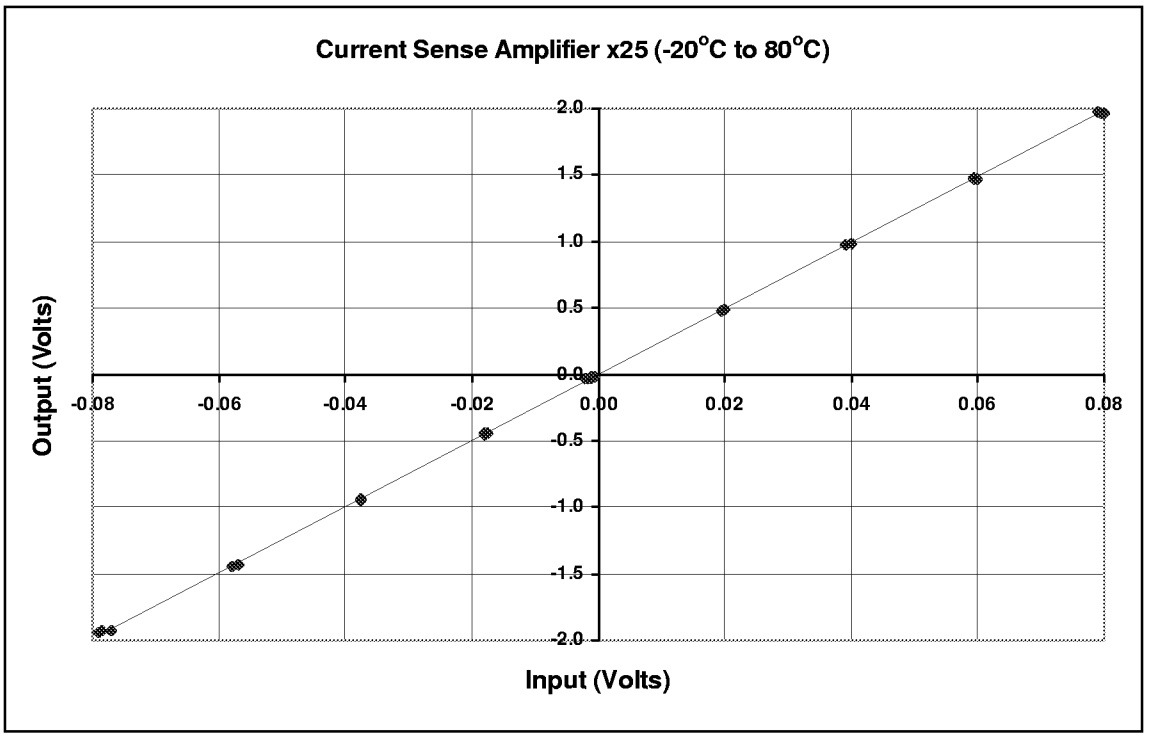




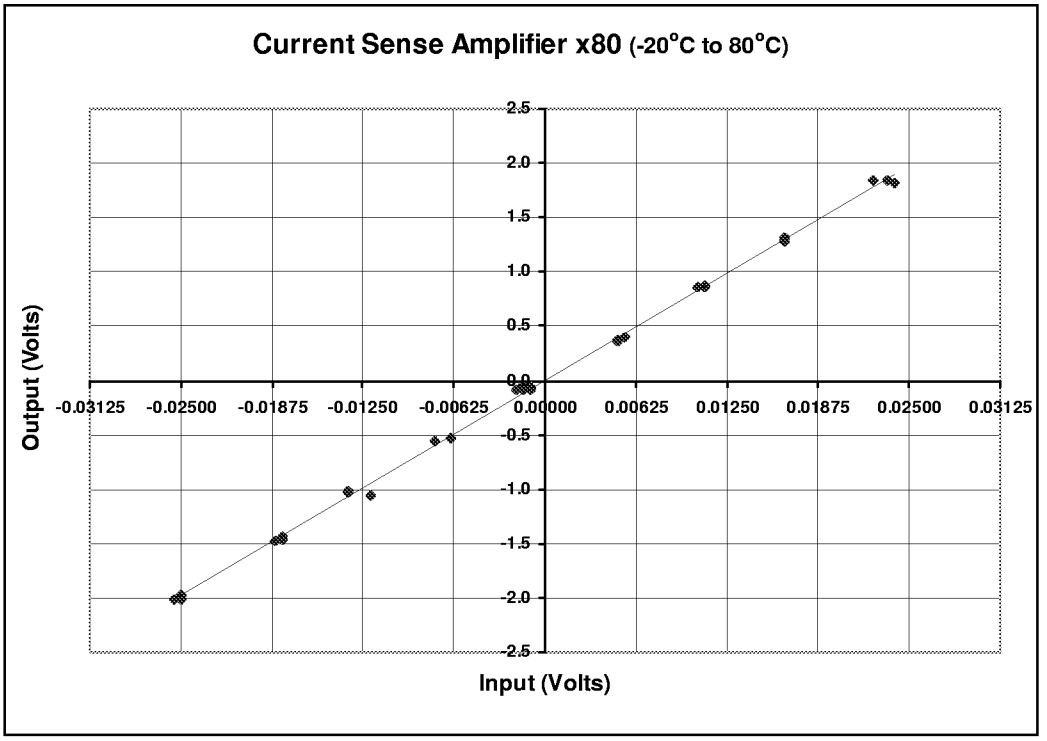


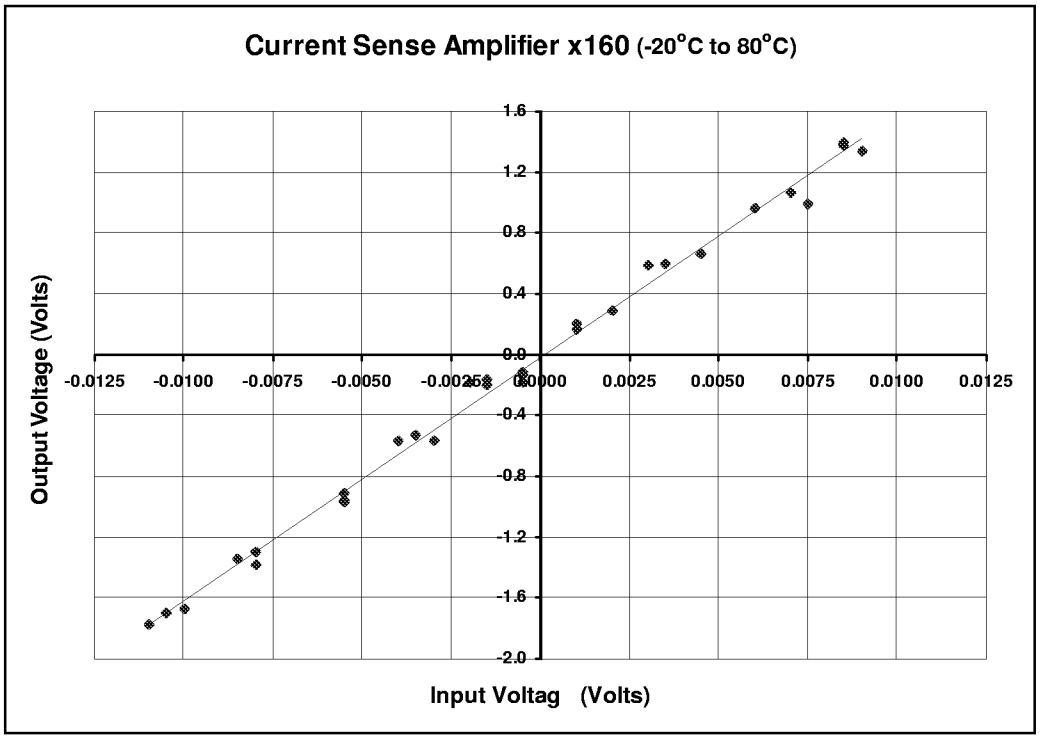
OVER VOLTAGE THRESHOLD



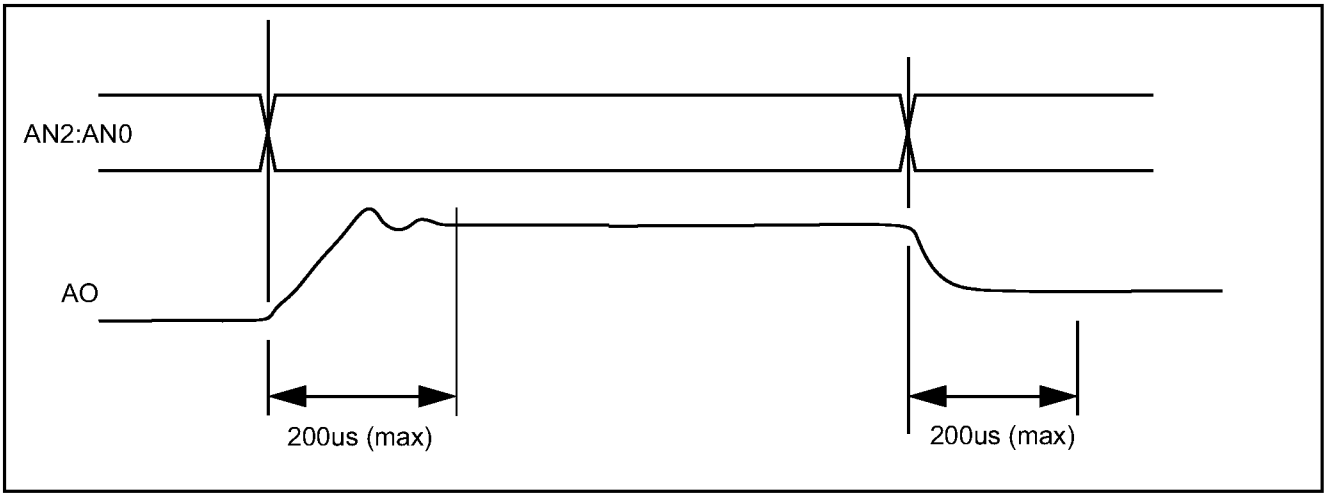


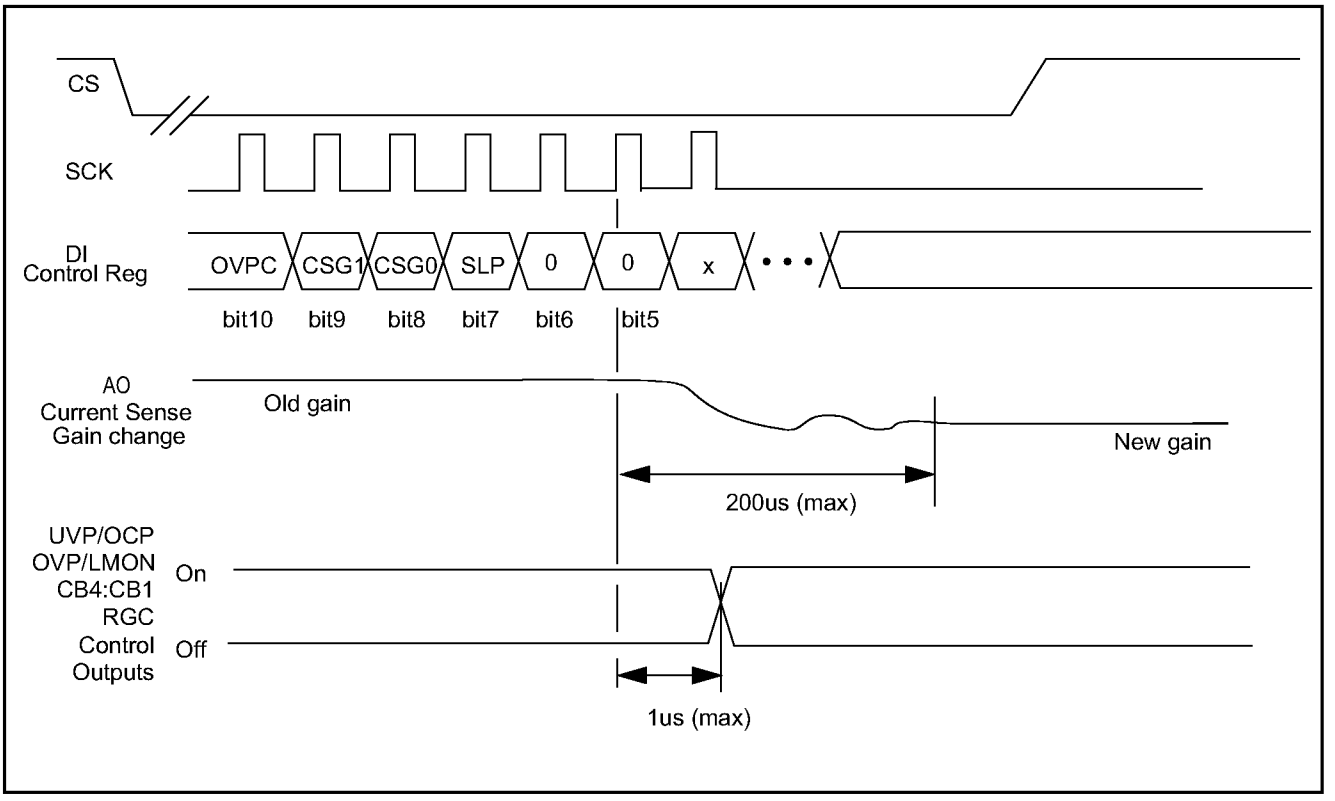
OVER VOLTAGE THRESHOLD



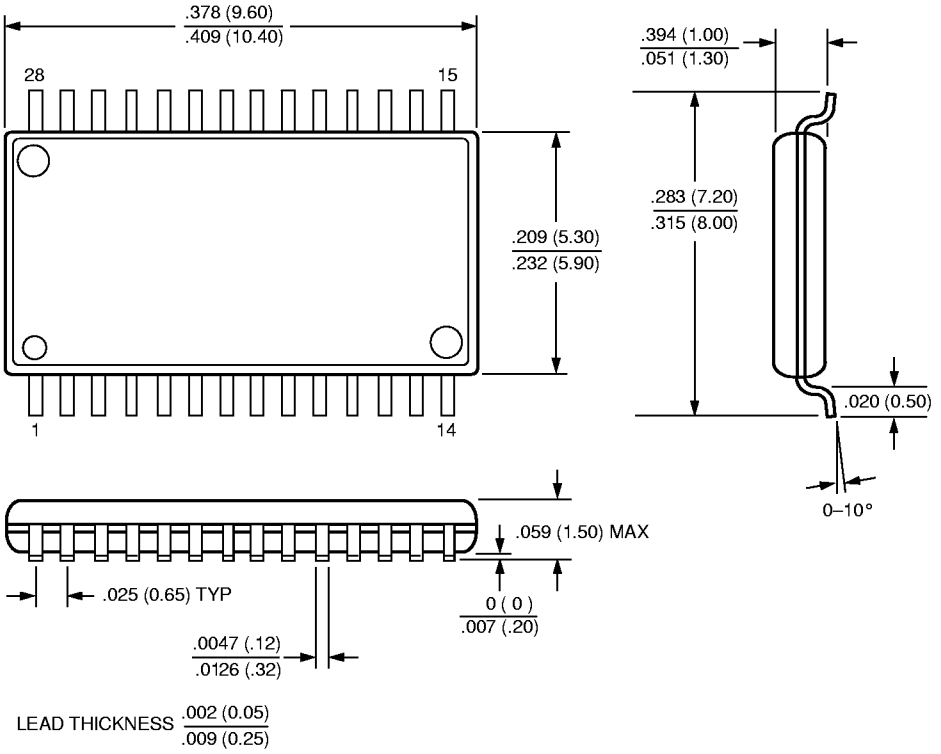


OVER VOLTAGE THRESHOLD

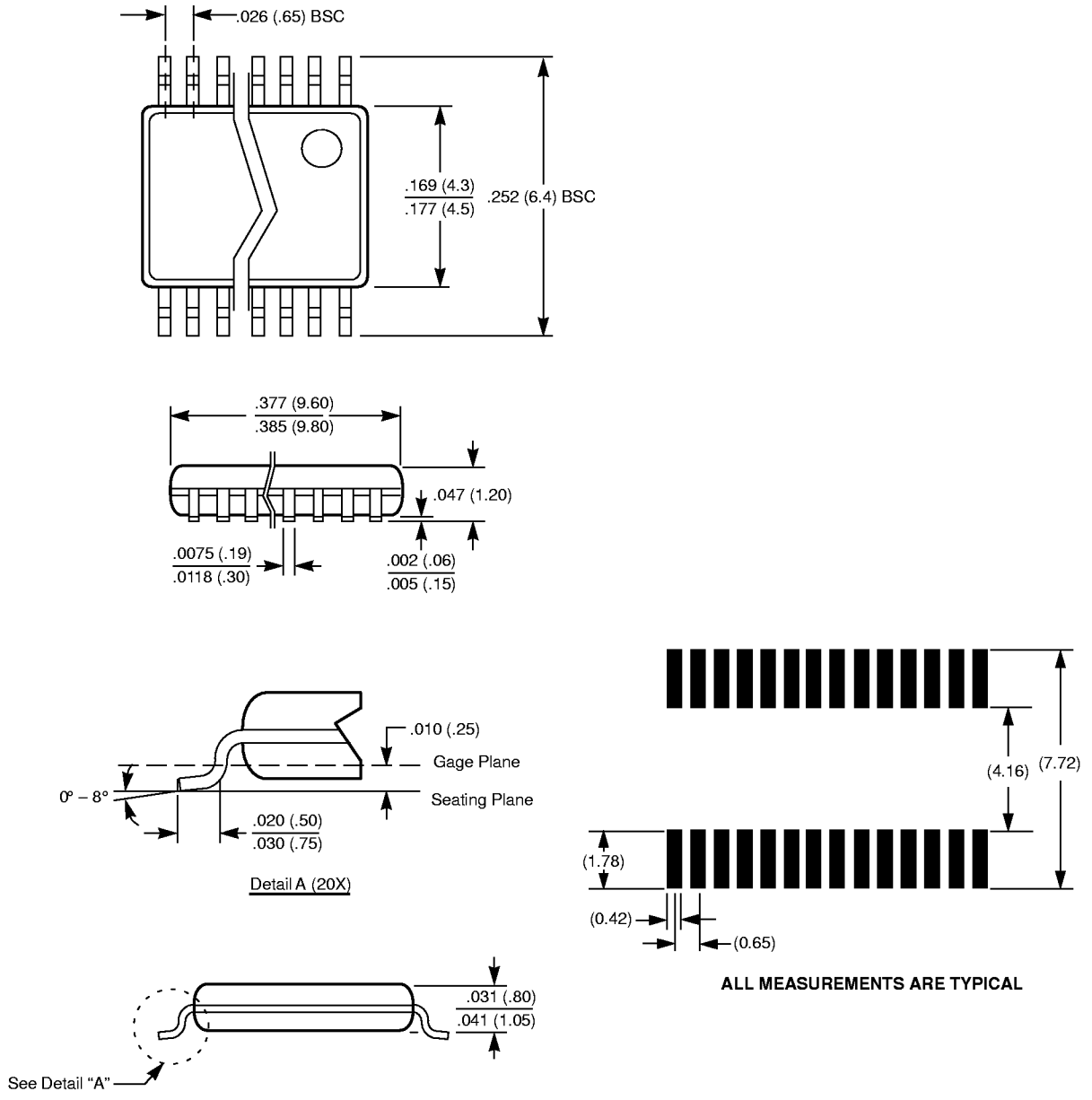




28-LEAD PLASTIC, SSOP, PACKAGE TYPE Q



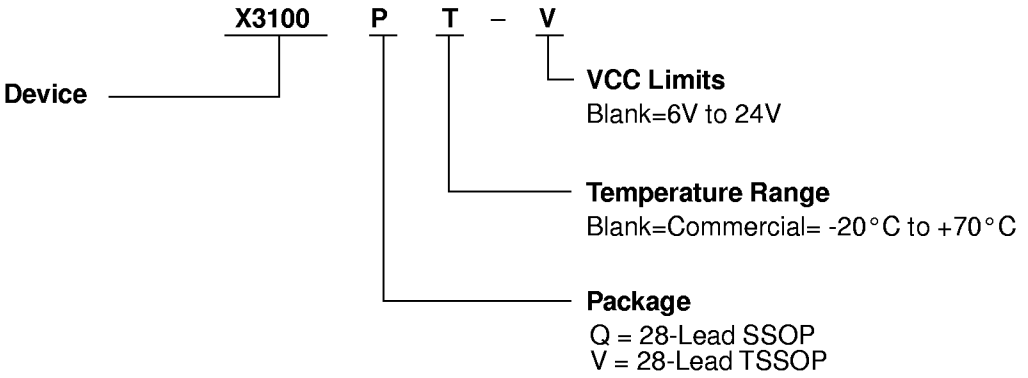
28-LEAD PLASTIC, TSSOP PACKAGE TYPE V



ALL MEASUREMENTS ARE TYPICAL

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

ORDERING INFORMATION



LIMITED WARRANTY

Devices sold by Xicor, Inc. are covered by the warranty and patent indemnification provisions appearing in its Terms of Sale only. Xicor, Inc. makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. Xicor, Inc. makes no warranty of merchantability or fitness for any purpose. Xicor, Inc. reserves the right to discontinue production and change specifications and prices at any time and without notice.

Xicor, Inc. assumes no responsibility for the use of any circuitry other than circuitry embodied in a Xicor, Inc. product. No other circuits, patents, licenses are implied.

U.S. PATENTS

Xicor products are covered by one or more of the following U.S. Patents: 4,263,664; 4,274,012; 4,300,212; 4,314,265; 4,326,134; 4,393,481; 4,404,475; 4,450,402; 4,486,769; 4,488,060; 4,520,461; 4,533,846; 4,599,706; 4,617,652; 4,668,932; 4,752,912; 4,829, 482; 4,874, 967; 4,883, 976. Foreign patents and additional patents pending.

LIFE RELATED POLICY

In situations where semiconductor component failure may endanger life, system designers using this product should design the system with appropriate error detection and correction, redundancy and back-up features to prevent such an occurence.

Xicor's products are not authorized for use in critical components in life support devices or systems.

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.